A 2.4 GHz Ultra-Low Power and High Gain Bulk Driven Mixer

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Abstract—A high gain, low voltage and ultra-low power double balance mixer using 0.18µm CMOS process is presented. For decreasing power consumption in this work, bulk driven technique with biasing transistors in sub-threshold region is used. The simulated results show maximum conversion gain of 32 dB at 2.4 GHz RF frequency, double sideband noise figure of 20 dB and IIP3 of +4 dBm while power consumption is only 15µW from 1.2 V supply voltage.

Keywords—bulk-driven, Gilbert cell mixer, sub-threshold, and voltage conversion gain.

I. INTRODUCTION

OWN conversion mixer plays an important role in any wireless receivers and divided to active and passive mixers. In recent years, double balance active mixers are favored due to good port to port isolation and higher gain [1]. Due to these reasons, conventional Gilbert cell mixer is commonly used.

Low voltage and low power design is required for mobile communication systems due to the limitation of battery capacity [2]. But Gilbert cell mixer has three stacked stages and therefore voltage supply isn’t low value.

Several techniques have been proposed to decreasing supply voltage and power consumption such as folded technique [3-5]. Folded technique is decoupling the bias current of the RF stage from LO stage [3]. Therefore, numbers of stacked transistors are reduced and voltage supply is decreased. But total current dissipation is increase and power consumption, dose not greatly reduce.

Another improvement technique is current reuse [6, 7]. In this technique, dissipated current in any stage is reuse in other stages. But due to stacked stages, voltage supply isn’t low value.

In this work, bulk driven technique [2, 8] and biasing transistors in sub-threshold region are used. In bulk driven technique, the bulk terminal of transistor will be used as controller terminal and RF or LO signal, depends on target of the performance, is connecting to it. This technique reduces of stacked transistors and therefore, voltage supply is decreasing. Also, the transistors biased in sub-threshold region for decreasing current dissipation. Therefore, power consumption of this work is ultra-low.

This paper is organized as follows. Details of this work presented in section II. Simulated results and comparison with other works are presented in section III and in section IV, the conclusion is summarized.

II. CIRCUIT DESIGN

In mixer design, the Gilbert cell mixer is base of many mixers due to benefits such as low even order distortion and good port to port isolation [9]. This mixer has three stacked stages as shown in Fig. 1. Also, RF and LO stages in this mixer operates in saturation region and as a result, power consumption is high.

![Circuit schematic of conventional Gilbert cell mixer.](image)

In proposed mixer, the transistor used as a four terminal device as shown in Fig. 2. Base of this work is bottom equation [2]:

\[
V_{TH} = V_{TH0} + \gamma \sqrt{2\phi_F} - V_{BS} - \gamma \sqrt{2\phi_F}
\]

(1)

where \(V_{TH0}\) is the zero substrate bias threshold voltage, \(\phi_F\) is the surface potential, \(\gamma\) is the body effect factor, and \(V_{BS}\) is the bulk to source voltage. LO signal is injected to gate and RF signal is injected to bulk of the transistors to modulate the
threshold voltage while the IF signal output was from the drain. Therefore, one stage is eliminated and voltage supply is lower than Gilbert cell mixer.

For decreasing current dissipation, M₁-M₄ are biased in sub-threshold region. In this region, drain current estimated by:

\[ I_D = \frac{W}{L} I_{D0} \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \]  

(2)

where \( W \) is width and \( L \) is length of the M₁-M₄, \( I_{D0} \) is a process-dependent factor, \( n \) is a sub-threshold slope factor, \( V_T \) is thermal voltage and \( V_{TH} \) is threshold voltage. Therefore, drain current is very low value because value of \( V_{GS} - V_{TH} \) is negative. In order to increasing conversion gain, PMOS active loads are used that operate in saturation region. Lauren’s expansion of exponential is obtained as follow:

\[ \exp(Z) = \sum_{n=0}^{\infty} \frac{Z^n}{n!} = 1 + Z + \frac{Z^2}{2} + \ldots \]  

(3)

Therefore, small signal drain current is equal to:

\[ i_d = \frac{W}{L} I_{D0} \left(1 + \frac{V_{gs} - V_{TH}}{nV_T} + \frac{1}{2} \left(\frac{V_{gs} - V_{TH}}{nV_T}\right)^2 + \ldots\right) \]  

(4)

From above terms, the third term is remains and other terms are eliminating by low pass filter.

\[ V_{gs} = k_1(\omega_{LO})A_{LO} \cos(\omega_{LO}t) \]  

(5)

\[ V_{bs} = k_2(\omega_{RF})A_{RF} \cos(\omega_{RF}t) \]  

(6)

where \( k_1(\omega_{LO}) \) and \( k_2(\omega_{RF}) \) are coefficients related to \( \omega_{LO} \) and \( \omega_{RF} \), respectively. \( \omega_{LO} \) is LO frequency, \( \omega_{RF} \) is RF frequency, \( A_{LO} \) and \( A_{RF} \) are amplitudes of LO and RF signals, respectively.

From (1), (5), and (6) and using from simplification:

\[ V_{gs} - V_{TH} = k_1A_{LO} \cos(\omega_{LO}t) + \frac{\gamma k_2A_{RF} \cos(\omega_{RF}t)}{2\sqrt{2} \phi_F} \]  

(7)

Therefore, small signal drain current after crossing the low pass filter is equal to:

\[ i_d = \frac{W}{L} \frac{I_{D0}}{I_{D0}} \frac{k_1k_2A_{LO}A_{RF}}{4nV_T^2} \cos(\omega_{IF}t) \]  

(8)

Therefore, voltage conversion gain can be calculated as follow:

\[ CG = \frac{V_{IF}}{V_{RF}} = \frac{W}{L} \frac{I_{D0}}{I_{D0}} \frac{k_1(\omega_{LO})k_2(\omega_{RF})A_{LO}Z_L(\omega_{RF})}{2nV_T^2} \]  

(9)

where \( Z_L(\omega_{RF}) \) is load equivalent impedance at the output and is related to IF frequency.

### III. SIMULATION RESULTS

This design simulated in 0.18 µm CMOS process in Agilent Design System package. In Table I, the size of transistors and values of other circuit elements are reported. M₁-M₄ are sized and biased so those operate in the sub-threshold region.

**TABLE I**  
Parameters values for proposed mixer.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_{1,4} )</td>
<td>26*2.5 µm</td>
<td>( R_{1,2} )</td>
<td>1 kΩ</td>
</tr>
<tr>
<td>( W_{5,6} )</td>
<td>3 µm</td>
<td>( R_{3,4} )</td>
<td>100 Ω</td>
</tr>
<tr>
<td>( C_{1,2} )</td>
<td>1.9 pF</td>
<td>( R_{5,6} )</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>( C_{3,4} )</td>
<td>0.8 pF</td>
<td>( L_1 )</td>
<td>2 nH</td>
</tr>
<tr>
<td>( C_{5,6} )</td>
<td>1 pF</td>
<td>( L_2 )</td>
<td>2 nH</td>
</tr>
<tr>
<td>VDD</td>
<td>1.2 V</td>
<td>( V_0 )</td>
<td>290 mV</td>
</tr>
</tbody>
</table>

Maximum voltage conversion gain is equal to 32 dB at 2.4 GHz RF frequency as shown in Fig. 3. In this simulation, RF and LO input powers are equal to -30 and 0 dBm, respectively and IF frequency is equal to 5 MHz. IIP3 is simulated by two tone test and equal to 4 dBm as shown in Fig. 4. Double sideband noise figure (DSB NF) is equal to 20 dB at 2.4 GHz RF frequency as shown in Fig. 5.

Power consumption in this work is only 15 µW because of biasing transistors in sub-threshold region and using from bulk-driven technique. In this region, process dependent factor \( I_{D0} \) and sub-threshold slope factor \( n \) approximately are equal to 1.1 µA and 1.8, respectively. Therefore, bias current of M₁-M₄, approximately are equal to 3.5 µA. Therefore, power consumption of this work is ultra-low value.
The comparison between this work and other works are presented in Table II. As can be seen in it, this work is ultra-low power, high gain, and high linearity in comparison with other works.

IV. CONCLUSION

An ultra-low power, low voltage and high gain mixer using from 0.18 µm CMOS technology for 2.4 GHz RF frequency is presented. In order to decreasing power consumption, bulk driven technique with biasing transistors in sub-threshold region are used and for increasing conversion gain, PMOS active loads are used.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Process</th>
<th>RF Frequency (GHz)</th>
<th>Conversion Gain (dB)</th>
<th>DSB NF (dB)</th>
<th>IIP3 (dBm)</th>
<th>Power Consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work</td>
<td>0.18 µm</td>
<td>2.4</td>
<td>32</td>
<td>20</td>
<td>+4</td>
<td>0.014</td>
</tr>
<tr>
<td>[2]</td>
<td>0.18 µm</td>
<td>0.5–7.5</td>
<td>5.7</td>
<td>15</td>
<td>-5.7</td>
<td>0.48</td>
</tr>
<tr>
<td>[7]</td>
<td>0.18 µm</td>
<td>4.2</td>
<td>10.9</td>
<td>11.5</td>
<td>-12</td>
<td>0.2</td>
</tr>
<tr>
<td>[8]</td>
<td>0.18 µm</td>
<td>0.5–6</td>
<td>6</td>
<td>12</td>
<td>0</td>
<td>0.28</td>
</tr>
<tr>
<td>[10]</td>
<td>0.18 µm</td>
<td>2.4</td>
<td>33</td>
<td>8.5</td>
<td>-14.5</td>
<td>1</td>
</tr>
<tr>
<td>[11]</td>
<td>0.18 µm</td>
<td>2.4</td>
<td>18</td>
<td>8</td>
<td>-</td>
<td>0.5</td>
</tr>
</tbody>
</table>
V. REFERENCES


