A Parallel-Connected High Voltage Multiplier for Non-Thermal Food Processing

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Abstract—In this paper, a parallel-connected high voltage multiplier is proposed for non-thermal food processing utilizing an underwater shockwave. The proposed multiplier consists of two positive multiplier blocks and two negative multiplier blocks. In the proposed multiplier, these multiplier blocks are operated in opposite polarity. By connecting these blocks in parallel, the proposed multiplier provides a high stepped-up voltage at high speed, where the output voltage across the output capacitor is generated by combining the outputs of these multiplier blocks. Concerning the proposed multiplier with six stages, simulation program with integrated circuit emphasis (SPICE) simulations and theoretical analysis using a four-terminal equivalent circuit are performed. The results of this study are as follows: 1) Settling time of the proposed voltage multiplier is less than 150ms when the output capacitance is 10μF and 2) the theoretical results are in good agreement with SPICE simulated results. The derived theoretical equations are effective to estimate the power efficiency and output voltages of the proposed multiplier.

Keywords—Cockcroft-Walton multipliers, High speed multipliers, Non-thermal food processing, Parallel-connected multipliers.

I. INTRODUCTION

RECENTLY, non-thermal food processing [1] is attracting much attention. Among others, we focus on non-thermal food processing utilizing an underwater shockwave [2], where a high-voltage electric discharge is used as the source of the shock wave. For this reason, several types of high-voltage generators have been proposed. Among others, one of the most famous high-voltage generators is the Cockcroft-Walton voltage multiplier (CWVM) [3]-[5]. In past studies, Iqbal proposed a symmetrical CWVM using a cascade rectifier circuit [4] and Besar et al. suggested a bipolar CWVM [5]. Unlike a high voltage transformer with high turn ratio, the CWVM can eliminate the requirement for the heavy core. However, due to the electrical impedance of capacitors in lower stages, the output voltage of the CWVM begins to sag according to the increase of the number of stages. Furthermore, the speed of the conventional CWVM [3]-[5] is slow, because the diode switch is controlled by a sinusoidal waveform supplied by a commercial power source. In the non-thermal food processing utilizing an underwater shockwave, the CWVM which exhibits not only high step-up gain but also high response speed is desirable to crush hard food.

In this paper, a parallel-connected high voltage multiplier is proposed for non-thermal food processing utilizing an underwater shockwave. The proposed multiplier consists of two positive multiplier blocks and two negative multiplier blocks. In the proposed multiplier, these multiplier blocks are connected in parallel and are operated in opposite polarity. By combining the output voltages of these multiplier blocks, a high output voltage across the output capacitor is generated. Furthermore, by controlling diode switches by two-phase rectangular pulses, the proposed voltage multiplier can achieve high speed operation. To confirm the validity of the proposed multiplier, simulation program with integrated circuit emphasis (SPICE) simulations and theoretical analysis using a four-terminal equivalent circuit are performed concerning the proposed multiplier.

II. CIRCUIT CONFIGURATION

A. Conventional Voltage Multiplier

Fig.1 shows the Cockcroft-Walton voltage multiplier (CWVM) with N stages (N=1, 2, ···) [3]. By converting a sinusoidal waveform supplied by a commercial power source, the conventional multiplier generates the following voltage:

\[ V_{out} \approx 2N(V_{in} - V_{th}). \quad (N=1,2,\cdots) \]  

In (1), \( V_{in} \) is the maximum value of an AC input voltage and \( V_{th} \) is the threshold voltage of the diode switch. As Fig.1 shows, the conventional CWVM can realize the simple circuit constitution. However, the speed of the conventional CWVM is slow, because the frequency of electric current is 50 Hz in Eastern Japan and 60 Hz in Western Japan.

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Fig. 1 Conventional Cockcroft-Walton voltage multiplier
B. Proposed Voltage Multiplier

Fig. 2 shows the proposed voltage multiplier. The proposed multiplier consists of four voltage multiplier blocks: two positive multiplier blocks and two negative multiplier blocks. First, the AC signal $V_{ac}$ is full-wave rectified by a full-wave rectifier. Then, the non-overlapped two-phase rectangular pulse $\Phi_1$ and $\Phi_2$ are generated by using the full-wave rectified voltage $V_{in}$. As Fig. 2 shows, the proposed multiplier has four states: State-$T_1$, State-$T_2$, State-$T_3$, and State-$T_4$. Finally, by controlling diode switches by $\Phi_1$ and $\Phi_2$, the proposed multiplier provides the following stepped-up voltage:

$$V_{out} = V_{po} - V_{mo},$$

where

$$V_{po} = (2N + 1)V_{in} - (2N + 1)V_{th},$$

and

$$V_{mo} = -2NV_{in} + (2N + 1)V_{th}. \quad (N = 1, 2, \ldots)$$

In (2), $V_{po}$ is the output voltage of the positive multiplier block and $V_{mo}$ is the output voltage of the negative multiplier block. In the proposed multiplier, the parameter $N$ is set to six to generate an output voltage about 3.5kV. Owing to high speed rectangular pulses and parallel-connected structure, the proposed multiplier can achieve high speed operation. Furthermore, the number of stages of the proposed multiplier is about a half of that of the conventional CWVM shown in Fig. 1. Therefore, the proposed multiplier can alleviate the sag of the output voltage.

III. THEORETICAL ANALYSIS

In this section, the property of the proposed voltage multiplier is analyzed theoretically. The theoretical analysis is performed by assuming the equivalent circuit of Fig. 3, because it is known that the general equivalent circuit of the single-input single-output SC DC-DC converter can be expressed by a four-terminal circuit [6]. In Fig. 3, $m_1$ and $m_2$ are the conversion ratio of ideal transformers and $R_{sw}$ is called the SC resistance. In the theoretical analysis, these parameters are derived by using instantaneous equivalent circuits without complex matrix calculations.

Fig. 4 shows the instantaneous equivalent circuits of the proposed multiplier. In Fig. 4, the diode switch is modeled by an ideal switch, an on-resistance $R_{on}$, and a threshold voltage source $V_{th}$. In the steady state, the differential value of electric charges in $C_{pk}^1$, $C_{pk}^2$, $C_{mk}^1$, and $C_{mk}^2$ (1, 2, ..., 2N) satisfies the following equations:

$$\Delta q_{1pk}^i = 0, \quad \Delta q_{2pk}^i = 0, \quad \Delta q_{1mk}^i = 0,$$

and

$$\Delta q_{2mk}^i = 0, \quad (k = 1, 2, \ldots, 2N)$$

where $\Delta q_{1pk}^i$ and $\Delta q_{2pk}^i$ (i=1, 2, 3, 4) denote electric charges of the $k$-th capacitor of the positive voltage multiplier blocks in the case of State-$T_i$. On the other hand, $\Delta q_{1mk}^i$ and $\Delta q_{2mk}^i$ denote electric charges of the $k$-th capacitor of the negative voltage multiplier blocks in the case of State-$T_i$. The interval of State-$T_i$ satisfies the following conditions:

$$T = T_1 = T_3 \quad \text{and} \quad T_2 = T_4 = \delta T,$$

where $T$ is the period of clock pulses and $\delta$ is the parameter to determine the time of State-$T_2$ and State-$T_4$.

In State-$T_1$, the differential values of electric charges in the input and output terminals, $\Delta q_{T_1, V_{in}}$, $\Delta q_{T_1, V_{po}}$, and $\Delta q_{T_1, V_{mo}}$, are expressed by

$$\Delta q_{T_1, V_{in}} = \Delta q_{T_1, V_{po}} - \Delta q_{T_1, V_{mo}}$$

(5)

and

$$\Delta q_{T_1, V_{po}} = \partial T_1^{2p+2N} + \Delta q_{T_1}^{2p},$$

(6)

$$\Delta q_{T_1, V_{mo}} = -\partial T_1^{2m+2N} + \Delta q_{T_1}^{2m}.$$
Fig. 4 Instantaneous equivalent circuits; (a) State-$T_1$, (b) State-$T_2$, (c) State-$T_3$, and (d) State-$T_4$

On the other hand, in State-$T_2$, the differential values of electric charges in the input and output terminals, $\Delta q_{T_2,V_{in}}$ and $\Delta q_{T_2,V_{po}}$, are expressed by

\[ \Delta q_{T_2,V_{in}} = 0, \]
\[ \Delta q_{T_2,V_{po}} = \Delta q_{T_2}^{po}, \] (8)

and \[ \Delta q_{T_2,V_{mo}} = \Delta q_{T_2}^{mo}. \] (9)

In the same way, the differential values of electric charges in State-$T_3$ and State-$T_4$ are expressed by

State-$T_3$: \[ \Delta q_{T_3,V_{in}} = \Delta q_{T_3}^{1p1} - \Delta q_{T_3}^{1p2} - \Delta q_{T_3}^{1pN+1} - \Delta q_{T_3}^{2p1} - \Delta q_{T_3}^{2mN+1} + \Delta q_{T_3}^{lm1}, \] (11)
\[ \Delta q_{T_3,V_{po}} = \Delta q_{T_3}^{2p2} + \Delta q_{T_3}^{po}, \] (12)

and \[ \Delta q_{T_3,V_{mo}} = -\Delta q_{T_3}^{lm2N} + \Delta q_{T_3}^{mo} \] (13)

State-$T_4$: \[ \Delta q_{T_4,V_{in}} = 0, \] (14)
\[ \Delta q_{T_4,V_{po}} = \Delta q_{T_4}^{po}, \] (15)

and \[ \Delta q_{T_4,V_{mo}} = \Delta q_{T_4}^{mo}. \] (16)

Using (5)-(16), the average input current and the average output current can be expressed as

\[ I_{in} = \frac{\Delta q_{V_{in}}}{T} = \sum_{i=1}^{4} \frac{\Delta q_{T_i,V_{in}}}{T} \] (17)

and \[ I_{out} = I_{po} = -I_{mo} \] (18)
where \( I_{po} = \frac{\Delta q_{v_{po}}}{T} = \frac{4}{T} \sum_{i=1}^{4} \Delta q_{T_i V_{po}} \) \quad (19)

and
\[
I_{mo} = \frac{\Delta q_{v_{mo}}}{T} = \frac{4}{T} \sum_{i=1}^{4} \Delta q_{T_i V_{mo}}.
\quad (20)
\]

In (17)-(20), \( \Delta q_{v_{in}}, \Delta q_{v_{po}}, \) and \( \Delta q_{v_{mo}} \) are electric charges in \( V_{in}, V_{po}, \) and \( V_{mo} \), respectively. Substituting (3)-(16) into (17)-(20), we have the relation between the input current and the output currents as follows:
\[
I_{in} = -(2N+1)I_{po} + 2NI_{mo},
\quad (21)
\]
where \( \Delta q_{v_{in}} = -(2N+1)\Delta q_{v_{po}} + 2N\Delta q_{v_{mo}}. \)

From (21), the conversion ratios in Fig. 3 are obtained as:
\[ m_1 = 2N+1 \quad \text{and} \quad m_2 = 2N. \]

Next, in order to derive the SC resistances \( R_{SC} \), the consumed energy in one period is discussed. From Fig. 4, the total consumed energy in one period can be expressed as:
\[
W_T = \sum_{i=1}^{4} W_{T_i} = W_{T_1} + W_{T_3} = 2W_{T_1},
\quad (22)
\]
where
\[
W_{T_1} = \left( \frac{\Delta q_{T_{p1}^2} - \Delta q_{T_{p2}^2}}{T_s} \right) R_d + \left( \frac{\Delta q_{T_{p1}^{N-1}} - \Delta q_{T_{p2}^{N-1}}}{T_s} \right) R_d
\]
\[
+ \left( \frac{\Delta q_{T_{p1}^{2n}}^2}{T_s} \right) R_d \frac{\Delta q_{T_{p2}^{2n}}^2}{T_s} \right) R_d
\]
\[
+ \left( \frac{\Delta q_{T_{p1}^{m1}}^2}{T_s} \right) R_d \frac{\Delta q_{T_{p2}^{m1}}^2}{T_s} \right) R_d
\]
\[
+ \left( \frac{\Delta q_{T_{p1}^{1m}}^2}{T_s} \right) R_d + \frac{\Delta q_{T_{p2}^{1m}}^2}{T_s} \right) R_d
\]
\[
+ \left( \frac{\Delta q_{T_{p1}^{m2}}^2}{T_s} \right) R_d + \frac{\Delta q_{T_{p2}^{m2}}^2}{T_s} \right) R_d
\]
\[
+ \left( \frac{\Delta q_{T_{p1}^{2m+1}}^2}{T_s} \right) R_d + \frac{\Delta q_{T_{p2}^{2m+1}}^2}{T_s} \right) R_d
\]
\[
+ \left( \frac{\Delta q_{T_{p1}^{m+1}}^2}{T_s} \right) R_d + \frac{\Delta q_{T_{p2}^{m+1}}^2}{T_s} \right) R_d
\]
\[
+ \left( \frac{\Delta q_{T_{p1}^{2m+1}}^2}{T_s} \right) R_d + \frac{\Delta q_{T_{p2}^{2m+1}}^2}{T_s} \right) R_d
\]
\[
+ \left( \frac{\Delta q_{T_{p1}^{m+1}}^2}{T_s} \right) R_d + \frac{\Delta q_{T_{p2}^{m+1}}^2}{T_s} \right) R_d
\].

Using (3)-(16), (23) can be rewritten as
\[
W_T = 2(2N+1)\left( \frac{\Delta q_{v_{po}}^2}{(1-2\delta)^2} \right) R_d + (4N+1)\left( \frac{\Delta q_{v_{mo}}^2}{(1-2\delta)^2} \right) R_{on}.
\quad (24)
\]
Here, the consumed energy \( W_T \) of Fig. 3 is obtained as
\[
W_T = \left( \frac{\Delta q_{v_{po}}}{T} \right)^2 R_{SC} \cdot T
\quad (25)
\]

Therefore, from (24) and (25), we have the SC resistances as follows:
\[
R_{SC} = \frac{2(2N+1)}{1-2\delta} \frac{R_d + 2(4N+1)^2}{1-2\delta} \frac{R_{on}}{R_{on}}.
\quad (26)
\]

Especially, when the parameter \( \delta \) is zero, (26) can be rewritten as
\[
R_{SC} = 2(2N+1)R_d + 2(4N+1)^2 \frac{R_{on}}{R_{on}}.
\quad (27)
\]

By combining (21) and (26), the equivalent circuit of the proposed voltage multiplier can be expressed by the following matrix:
\[
V_{in} - \frac{2(N+1)}{4N+1} V_{th} = \left[ \frac{1}{4N+1} \frac{0}{4N+1} \right] \left[ \frac{1}{R_{SC}} \frac{0}{R_{SC}} \right] \left[ \frac{V_{out}}{V_{out}} \right]. \quad (28)
\]

Therefore, when the output load is the resistive load \( R_{L} \) and the power efficiency \( \eta \) and the output voltage \( V_{out} \) are expressed as
\[
\eta = \left[ \frac{R_L}{R_L + R_{SC}} \right] \left[ \frac{4N+1}{V_{in}} - \frac{2(N+1)}{4N+1} V_{th} \right]
\quad (29)
\]
and
\[
V_{out} = \left[ \frac{R_L}{R_{L} + R_{SC}} \right] \left[ (4N+1) V_{in} - 2(2N+1) V_{th} \right]. \quad (30)
\]

IV. SIMULATION

To clarify circuit characteristics, SPICE simulations are performed concerning the proposed voltage multiplier with six stages. First, the property of the proposed voltage multiplier is compared with that of the conventional CWVM shown in Fig. 1.

Fig. 5 shows the simulated output voltage. In Fig. 5 (a), the SPICE simulations were performed under conditions that \( V_{AC} = 100V @50Hz, T = 100\mu s, T_i = 49.9\mu s, \delta = 0.001, C_{p1} = C_{p2} = C_{out} = 10\mu F, C_{in} = 1\mu F, \) and \( C_{in} = 10\mu F. \) On the other hand, in Fig. 5 (b), the simulation conditions are as follows: \( V_{AC} = 100V @50Hz, C_i = 10\mu F, \) and \( C_{out} = 10\mu F. \) The simulated voltage multiplier was designed by using the diode model MUR460 and the capacitor model with 0.001\( \Omega \) internal resistance. As Fig. 5 shows, the proposed multiplier can generate an output voltage at high speed. Concretely, the settling time of the proposed multiplier is less than 150ms. On the other hand, the settling time of the conventional CWVM is about 130 seconds.

Next, to confirm the validity of the theoretical analysis described in Sect. 3, the SPICE simulations are performed. Fig. 6 shows the comparison between simulated efficiency and theoretical efficiency. Fig. 7 shows the comparison between simulated outputs and theoretical outputs. In the SPICE simulation of Figs. 6 and 7, the diode switch was modeled by an
V. Conclusion

For non-thermal food processing utilizing an underwater shockwave, a parallel-connected high voltage multiplier has been proposed in this paper. The validity of circuit design was confirmed by SPICE simulations and theoretical analysis.

The result of SPICE simulations showed that the proposed multiplier can achieve higher speed than the conventional Cockcroft-Walton voltage multiplier. Concretely, the settling time of the proposed multiplier with six stages is less than 150 ms when the output capacitance is 10\( \mu \)F. On the other hand, the settling time of the conventional voltage multiplier is about 130 seconds when the output capacitance is 10\( \mu \)F.

Concerning the output voltage and power efficiency, handy theoretical equations were derived by using a four-terminal equivalent circuit. These theoretical results were in good agreement with SPICE simulated results. Therefore, the formulas obtained by the theoretical analysis will be helpful to design the proposed voltage multiplier.

REFERENCES


