Data-Weighted Averaging Technique for Sigma-Delta ADC with Segmented DAC

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Abstract—Data weighted averaging algorithm work well for relatively low quantization levels, it begin to present significant problems when internal quantization levels are extended farther. Each additional bit of internal quantization causes an exponential increase in the complexity, size, and power dissipation of the DWA logic and DAC. This is because DWA algorithms work with unit-element DACs. The DAC must have 2^N−1 elements (where N is the number of bits of internal quantization), and the DWA logic must deal with the control signals feeding those 2^N−1 unit elements. This paper discusses the prospect of using a segmented feedback path with coarse and fine signals to reduce DWA complexity for modulators with large internal quantizers. However, it also creates additional problems. Mathematical analysis of the problems involved with segmenting the digital word in a ΣΔ ADC feedback path are presented, along with a potential solution that uses frequency-shapes this mismatch error. A potential circuit design for the frequency-shaping method is presented in detail. Mathematical analysis and behavioral simulation results are presented.

Keywords— Sigma-Delta, data weighted averaging (DWA), Segmentation

I. INTRODUCTION

The sigma-delta analog to digital converter (ΣΔ ADC) has been widely used in recent decades for low frequency, high resolution (even up to 24 bit) applications such as digital audio and high-precision instrumentation[2],[8]. Recent work, however, is extending the signal bandwidths of ΣΔ ADCs into the MHz range while maintaining high resolution [5].

There are three ways to increase the resolution of a sigma delta modulators. one can increase the sampling frequency relative to the bandwidth of interest, the order of the noise transfer function, and the number of internal quantization levels. All three of these approaches come with an attendant cost in power dissipation, the complexity and circuit area. Early ΣΔ converter used a single bit quantizer in the loop[3],[4] because of their suitability for VLSI implementation and their superior linearity. The use of multibit quantization has been limited because non linearity in the DAC of a sigma-delta modulator translates directly into non linearity of the entire modulator, producing a distorted output. Non linearity in the DAC also modulates the quantization noise into the signal band, thus degrading the SNR. However, multibit modulators have several advantages such as increased resolution for the same oversampling ratio, improved stability, relaxed amplifier requirements and better tone behaviour.

 Attempts to eliminate the non linearity problem associated with multibit ΣΔ modulators have resulted in the use of DWA techniques which shape the noise generated by DAC unit element mismatch, shifting it to higher frequencies which are out of the band of interest.

Increasing internal quantization levels beyond five bits improves SNR but presents significant challenges. Both the internal quantizer and the DWA logic grow exponentially in complexity, size, and power dissipation as the internal quantizer resolution increases.

Using a coarse/fine ADC is a logical alternative for reducing quantizer power. A folding ADC could provide quantization above eight bits while still maintaining the low latency required of the internal quantizer. Recent work has also shown that it is possible to incorporate two-step ADCs with in a single loop modulator, permitting lower power quantizers while maintaining loop stability [12], [13].

This paper will present an architecture that permit the uses of DWA with a coarse/fine quantizer. The paper is organized as follow. In section II, reviews data weighted averaging technique for modulators ΣΔ ADC. In section III, the proposed method of segmentation is described. In section IV, the problem segmented coarse/fine DAC structure is discussed. In section V, method requantization to overcome this problem is presented. Simulation results are shown to demonstrate this method’s performance.

II. THE DATA WEIGHTED AVERAGING ALGORITHM (DWA)

Multi bit quantization improves the stability and the signal-to-quantization noise performance of sigma-delta converters, but it also necessitates the use of dynamic element matching (DEM) to filter the nonlinearity error in the signal band. Data weighted averaging (DWA) is the most widely used DEM algorithm, due to its simplicity and low hardware overhead.

The basic concept of DWA is to guarantee that each of the elements is used with equal probability for each digital input code. This is realized by sequentially selecting elements, beginning with the next available unused element. The operation principle is illustrated in Fig 1. v(n) denotes the
DAC input at clock cycle n. In the 1st clock four unit elements are selected. Then in the next clock the elements are selected from the first unused, that is the 5th element. If the last element is selected, DWA will start to select the 1st one again. DWA shapes the nonlinear errors with the first-order transfer function \(1-z^{-1}\) [7].

DWA WITH SEGMENTED QUANTIZER

A folding or two-step architecture for the internal quantizer can solve some of the problems arising from increasing the internal quantization level beyond 5 bits. Since these architectures provide the digital data in two sections, coarse bits and fine bits, a logical way to interface with the DWA is to simply perform DWA independently on the coarse and fine DAC banks, as illustrated in Fig 2. The quantizer produces \(N_C\) bits as the coarse signal and \(N_F\) bits as the fine signal, for a total of \(N\) bits \((N = N_C + N_F)\). Fig 3 shows a mathematical representation of the segmented architecture from Fig 2.

The two-step quantizer resolves the \(N_C\) coarse bits, and then subtracts this value from the input and generates the \(N_F\) fine bits from this signal. The gain of \(2^{-(N-N_C)}\) inside the quantizer represents a binary right shift to insure the correct place value of the bits, since the coarse bits are the \(N_C\) most significant bits of an \(N\) bit signal. Since DWA shapes the error due mismatch unit element DAC with first order transfer function, the DWA blocks can be represented as \((1-z^{-1})\), as seen in Fig 3. The coarse and fine outputs are each applied to separate DACs using smaller, independent DWA circuits, reducing DWA complexity significantly. The coarse DAC transfer function is weighted by \(2^{N-N_C}\) times that of the fine DAC to insure that the original place values are preserved. However, since this weighting depends on the size of the unit elements involved, a gain mismatch, \(1-c\), will be present. The quantization noise, \(Q_C\), present in both signals \(Y_C\) and \(Y_F\), ideally will cancel when the coarse and fine signals are summed together at the modulator input. This result should be the same as if a single DWA circuit with a single DAC had been in the feedback path. However, because of the gain mismatch between the DACs, the coarse quantization error will not completely cancel and will be transmitted to the output.

\[
Y(z) = Y_c(z)2^{N-N_C} + Y_F(z) \\
(1)
\]

Where

\[
Y_C(z) = \frac{2^{-(N-N_C)}[Q_C(z) + (X(z) - (1 - Z^{-1})Y_F)H(z)]}{1 + (1-c)(1-Z^{-1})H(z)} \\
(2)
\]

And

Fig 1. The DWA operation principle

Fig 2. Block Diagram of Segmented ∆Σ ADC

Fig 3. Mathematical Block Diagram of Segmented ∆Σ ADC
\[ Y_F(z) = -Q_C(z) + Q_F(z) \]

by substituting (2) and (3) into (1), it is obtained as follows:
\[ Y(z) = \frac{X(z)H(z)}{1 + (1-\varepsilon)(1-z^{-1})H(z)} + \frac{Q_F(z)}{1 + (1-\varepsilon)(1-z^{-1})H(z)} + \frac{\varepsilon(1-z^{-1})}{1 + (1-\varepsilon)(1-z^{-1})H(z)}(Q_C(z) - Q_F(z)) \]
\[ (4) \]

For comparison, a non-segmented (single-path) approach would lead to:
\[ Y(z) = \frac{X(z)H(z)}{1 + (1-z^{-1})H(z)} + \frac{Q(z)}{1 + (1-z^{-1})H(z)} \]
\[ (5) \]

A comparison of Equations (4) and (5) shows that the segmented system has the error term \( \varepsilon \cdot (Q_C - Q_F)(1-z^{-1}) \) present in addition to normal quantization noise. The value of the mismatch term, \( \varepsilon \), changes with each clock cycle due to the operation of the DWA. For realistic unit-element mismatch values, \( \varepsilon \) is small, but still large enough to significantly affect the SNR of the system. Fig 4 shows the output spectrum for both non-segmented and segmented systems for a second order modulator with an OSR of 32 and 1% element mismatch. The non-segmentation represents a DAC with 8-bit DWA. For the segmentation system and 1% mismatch, using independent coarse/fine DWA results in a 20 dB degradation in SNR from the non segmented case.

V. THE NOISE-SHAPED REQUANTIZATION (ReQ) METHOD

The mismatch error between coarse and fine banks can be noise shaped if the coarse quantization is performed within a digital ΣΔ modulator. This method was initially proposed in [17] for a ΣΔ DAC, then this method in [16] was proposed for ΣΔ ADC along DEM with gain of unity. This work extends this concept to ΣΔ ADCs with DWA algorithms.

The basic idea is to generate a new coarse signal with a digital ΣΔ modulator and use this coarse signal to generate a new fine signal. This insures that both the coarse and fine signals are individually noise shaped, which is performed in a way that causes the quantization error leakage to be noise shaped as well. Even though it does not completely cancel errors due to DAC mismatch, the quantization error noise power will be outside the signal band. The process is modeled in Fig 5. Fig 6 shows a mathematical representation of the ReQ architecture from Fig 5. The digital coarse and fine signals from the quantizer are first concatenated to form an \( N \)-bit signal. This signal is then requantized to \( N_C \) bits using a digital first-order ΣΔ modulator. Then coarse signal is subtracted from the original \( N \)-bit signal to form the new fine signal, comprised of \( N_F+1 \) bits. After requantization, the new coarse and fine signals become:

\[ Y_C'(z) = 2^{-(N-N_C)}[Y(z) + Q_C'(z)(1-z^{-1})] \]
\[ (6) \]
\[ Y_F'(z) = -Q_C'(z)(1-z^{-1}) \]
\[ (7) \]

Signals \( Y_C'(z) \) and \( Y_F'(z) \) then pass through independent DWA blocks and DACs and are summed at the input of the modulator. With first-order requantization (ReQ), the quantization error that is not completely cancelled due to coarse/fine DAC mismatch as in Equation (4) is noise-shaped away from the signal band. The output of the system with ReQ as in Fig 6 is derived as follows:
\[ Y'(z) = Y_C(z)2^{N-N_C} + Y_F(z) \]
\[ (8) \]
Where
\[ Y_C(z) = 2^{-(N-N_C)} [Q_C^t(z) + (X(z) - (1-\epsilon)(1-z^{-1})2^{N-N_C} Q_C(z)] - Y_F(z)(1-z^{-1}))H(z)] \]

And
\[ Y_F(z) = -Q_C(z) + Q_F(z) \]

By substituting (9) and (10) into (8), it is obtained as follow:
\[ Y'(z) = \frac{X(z)H(z)}{1+(1-\epsilon)(1-z^{-1})H(z)} Q_F(z) + \frac{(\epsilon Q_C(z))(1-z^{-1})^2 H(z)}{1+(1-\epsilon)(1-z^{-1})H(z)} \]

Which shows that the coarse quantization noise leakage is first-order shaped. Fig 7 shows the output spectrum for ReQ method. again 8bit two-step quantizer, second order modulator with OSR of 32 was used. Table 1 shows simulated results. First row is the SNR of non segmented \( \Sigma\Delta \) ADC at various unit-element mismatch values. The second row shows the segmented case. The third row shows the ReQ case. At 1\% mismatch, the segmented ADC has an SNR 20 dB lower than the non-segmented case. In comparison, the ADC with ReQ has an SNR only 2 dB lower than the non segmented case.

III. CONCLUSION

The DWA algorithm modulates the nonlinearity of the DAC due to mismatch unit element, moving the harmonic distortion out of the signal bandwidth, which can be removed by the digital low-pass filter in the following stage.
A segmented architecture with coarse/fine DAC and DWA combined with the ReQ method has been proposed to reduce the complexity of DWA and DAC due to the large number of bits used in the internal quantization. The ReQ method proposed in this paper allow for larger internal quantizers without the exponential increase in DWA and DAC circuits, while still maintaining performance close to the one quantizer with DWA system.

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