**Abstract**—This paper introduces a new method for introducing Membership function in fuzzy systems. And a new high-speed analog fuzzification circuit was introduced for implementing this idea and verified by simulations. It is characterized by a trapezoidal membership function with independently adjustable parameters. The core of the circuit is a BiCMOS current-mode circuit which works as a fuzzifier. The addition of rectifying linear voltage to current converters allows its utilization as a voltage-mode fuzzifier. This scheme is expected to find application in neuro-fuzzy processors where adaptation of the membership function parameters is required. The result is a faster, cheaper and higher controllable compare to conventional fuzzification techniques.

**Keywords**—Fuzzifier, BiCMOS, Mixed-Mode, Membership function, soft controlling

I. INTRODUCTION

**FUZZY** logic is an innovative technology to provide engineering systems with human expertise [1]. It is being used in many applications that include industrial automation, process control and data processing.

Fuzzification is the basic operation of fuzzy logic. It is used to determine the degree of membership of a system's input and output variables to fuzzy sets.

Membership functions are characterized by degree of association curves. One of the most common shapes is the trapezoidal function (Fig. 1). This function includes triangular, S- and Z-shaped functions as Fig. 1 Trapezoidal membership function special cases.

![Trapezoidal membership function](image)

**Fig. 1 Trapezoidal membership function**

Special purpose fuzzy processor chips have been developed for applications that require high speed. Most fuzzy processors chips are based on digital techniques. Digital implementations are silicon area intensive, but they have the advantage of easy programmability and easy interfacing to conventional digital systems. Analog approaches are inherently faster and require much smaller silicon area and lower power consumption [5]-[6]. Their main disadvantage is that they are not so easily programmable. In this paper we present a new high-speed current-mod/voltage-mode fuzzifier characterized by a trapezoidal membership function (Fig. 1). The x-position of the corners (Va, Vb, Vc, Vd) of the trapezoidal function as well as its amplitude (Vamp) are independently and continuously adjustable. This feature is specially useful for high speed neuro-fuzzy applications (7).

Artificial Neural Networks (ANNs) enjoy some distinguished characteristics and are composed of simple elements operating in parallel and including the ability to learn from data, to generalize patterns in data, and to model nonlinear relationships. These elements are inspired by biological nervous systems. As in nature, the network function is determined largely by the connections between elements. We can train a neural network to perform a particular function by adjusting the values of the connections (weights) between elements. These appealing features make neural networks a good candidate for overcoming some of the difficulties in traditional devices and circuit modeling and optimization. Because of these, recently neural networks have become a much important way in nonlinear modeling of devices, signal processing, robotic systems, code sequence prediction, integrated circuit chip layout, process control, chip failure analysis, process control, chip failure analysis, machine vision, voice synthesis, spiking, and more [4, 6, 7, 8 and 10].

The fuzzifier presented in this paper suitable circuit to analyze and tune the nonlinear parameters of membership functions. These techniques provide a method for the fuzzy modeling procedure to learn information about a data set, in order to compute the membership function parameters that best allow the associated fuzzy inference system to track the given input/output data. This learning method works similarly to that of neural networks. Our discussions are started with summery of Nero-Fuzzy structures and back propagation algorithm and then describing BiCMOS structure along with circuit designs of fuzzifier.
II. NERO-FUZZY ARCHITECTURE

Functionally the Nero-Fuzzy architecture is the major training routine equivalent to Takagi-Sugeno first order fuzzy inference systems (FIS)[2]. Anfis uses a hybrid learning algorithm to identify parameters of Sugeno-type FIS. It applies a combination of the least-squares method and the back propagation gradient descent method for training FIS membership function parameters, to emulate a given training data set. In other words to start Anfis learning, first a training data set is required that contains desired input/output data pairs of the target system to be modeled. The Anfis structure used to implement fuzzy controller with five layers is shown in Fig. 1. It consists of two inputs, four membership functions for each input, sixteen fuzzy rules and one output. The Anfis applies fuzzy inference techniques to data modeling. According to this structure, the shape of the membership functions depends on parameters, so changing these parameters will change the shape of the membership functions. The benefit of this method is that it chooses the membership function parameters automatically, that’ better than just monitoring the data and estimate these parameters.

III. PROPOSED CIRCUITS

According to the figure 2, to create the layers 1 and 2, we proposed a new CMOS membership function generator which has differential pair structure with analog voltage crisp input and analog current outputs (Fig. 2).

This circuit is capable of making three types of Gaussian, Trapezoidal and Triangular shapes in comparison with before works [9, 11, 12 and 14]. After Anfis training and choose suitable shape and slopes membership functions, we can adapt our Fuzzifier circuit using voltage references and switch controllers to tune type and slope of shapes respectively. The new fuzzifier uses two types of cells equation, linear voltage to current converter (LVCC) circuits and Gilbert translinear piecewise-linear transconductance characteristic shown in Fig. 4. The output current, $I_{out}$, is zero for negative input voltages $V_i < 0$ (where $V_o = V_I - V_d$). It has a linear-region with constant slope $s = I/R$ for $0 < V_i < -d$, and it saturates with a current $I$, for $V_i > I$ (R). For $V_i < 0$ the differential-pair current flows through transistor $M_{catch}$. This transistor works similar to a catch diode: it provides a path for negative currents to flow and prevents large voltage swings at the output node of the differential pair. This avoids degradation of the speed of the circuit Fig. 3 shows the utilization of two LVCCs to produce the transconductance characteristic of Fig. 3. This has a linear region in the range $V_o < V_m < V_s$. The left LVCC is used to set the bias (saturation) current of the right LVCC to a value $I_m = (V_s - V_o)/R$. The output current of the right LVCC has the transconductance characteristic shown in Fig. 3 with a linear region in the range $V_o < V_m < V_s$, slope $s = I/R$ and saturation current $I_m = (V_s - V_o)/R$. A similar Arrangement is used to produce a Transconductance Characteristic with a linear region $V_o < V_m < DVD$ and with saturation current (for $V_m > DVD$) $I_m = (V_s - V_o)/R$. Fig. 3 shows the utilization of two GTCs to generate currents $I_m$ and $I_{amp}$ that have saturation currents lamp and with linear regions in the ranges $V_o < V_m < V_s$ and $V_o < V_m < V_d$ respectively. The GTC is current multiplier/divider 18.

It is characterized by the expression $I_{out} = I_{in}/I_{amp}$ where 11, 12, 13 and 14 are the collector currents in $Q_3, Q_5, Q_7$ and $Q_8$ respectively. In Fig 4, for the left GTC $I_{out} = (V_m - V_o)/R$, $I_{out} = (V_o - V_s)/R$ and $I_{out} = I_{amp}$. The output current is given by $I_{out} = I_{out} = I_{amp}(V_m - V_o)/R$. It has the piecewise linear characteristic shown on the left of Fig. 4. The left GTC in Fig. 4 is used to generate an output current $I_{out}$ with the piecewise linear characteristic shown in Fig. 3 (middle). This has an anti-ut saturation current lamp (for $V_m > V_d$) and $I_{out} = I_{amp}(V_m - V_o)/R$. A current mirror is used to generate the overall output current $I_{out}$ that has the trapezoidal characteristic of Fig. 1 with independently adjustable parameters: $V_m, V_o, V_s, V_d$ and lamp=$V_{amp}/R$. Variables and parameters can be defined in the current domain according to, $I_{amp} = V_{amp}/R$, $I_o = V_o/R$, $I_s = V_s/R$, $I_m = V_m/R$, $I_{out} = V_{out}/R$. The LVCC circuit is shown in Fig 4. Proposed BiCMOS Fuzzifier.
$l_b=\frac{V_b}{R}$, $l_a=\frac{V_a}{R}$ and $l_c=\frac{V_c}{R}$. In this case the circuit of Fig. 3 alone can be considered a current-mode fuzzifier. Currents $l_{na}$, $l_{amp}$, $l_{io}$, and $l_{o}$ can be replicated (and rectified) using current mirrors.

IV. RESULTS

HSPICE simulations using 2pm BiCMOS technology N-well parameters (MOSIS) were performed. P and N transistors with dimensions 24/2 and 12/2 (in pm) were used for the simulations. Fig. 7 shows the HSPICE simulated transfer characteristic of the LVCC circuit of Fig. 7. The high speed rectifying characteristic can be verified with the transient response to a 4V, 10MHz sinewave signal. Fig. 7 shows the trapezoidal DC transfer characteristic of the overall circuit for $V_c=0V$, $V_a=0.75V$, $V_b=1.75V$ and $V_d=3V$.

A breadboard prototype of the fuzzifier was implemented using commercial bipolar OTAs (CA3280). These OTAs have a GTC between their input terminals. External resistors R in series with the input terminals are used for linearization and to extend the input range of the OTA. The output current of the OTA is expressed by $I_{out}=I, V_{o}=2R$ in its linear region.

The systematic model of controller was evaluated using Anfis architecture training. To start training an FIS, first we need to have a training data set that contains desired input/output data pairs of the target system to be modeled. Sometimes we should have the optional testing data set that can check the generalization capability of the resulted FIS. Therefore the checking data set helps with model over fitting during the training. The next stage is to specify initializing and generating of FIS parameters for Anfis training. In this paper we initialize the FIS with two inputs which one of them has four Gaussian and the other one has four Trapezoidal shapes, sixteen rules and one output. After training, the improved and changed membership functions are obtained and shown in figure 4. The total extracted control surface of controller is introduced and illustrated in figure 5 too.
controller. The simulation results and extracted control surfaces show the good compatibility, adapted and the same of Anfis training and hardware results of FLC chip with high accuracy. Simulation results that verify the operation of the fuzzifier are presented.

ACKNOWLEDGMENT

The authors would like to thank Islamic Azad University; Mahabad branch for funding this research.

REFERENCES

[13] Sadeq Aminifar - (Born 1975) received his B.S. in 1999 in Electrical Electronics Engineering from the Shahid Beheshti University, Tehran, Iran and his M.S. in 2002 in Electronics Engineering from the Urmia University, Urmia, Iran. He was the Teaching Assistant of Electrical Engineering Department of the Urmia University since 1999 to 2002.
[14] M. Daneshvar - (born 1975) was born in Urmia, Iran. He received B.S. degree in electrical Electronics engineering from the University of Urmia, Urmia, Iran in 1996. And M.S. Degree in electrical Electronics engineering from the University of Science and Research of Islamic Azad University, Tehran, Iran. in 2007. He is PhD student since 2011. His primary research interest was analog circuits. Fuzzy controller, intelligence IC. Recently, his research has involved digital circuits with emphasis on high-performance digital circuits and neural network.
[15] Ghader Yosefi - was born in 1980. He received his B.S. degree and M.S. degree in electrical engineering from the Urmia University, Urmia, Iran. in 2002, 2007 respectively. He works on Mixed-Mode fuzzy logic controllers and data converters at the Urmia Microelectronic Research Center and Electronic Lab of Mahabad Azad University since2002.