Design of High-speed Video Transmission Interface for 3D TV

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Abstract—High definition 3D video is used in various electronic devices such as digital camera, video game and TV. To support transmission of 3D device, HDMI is suitable as an interface between video source and sink due to its low noise and high speed connection. In this paper, we design HDMI transmitter and receiver for stereo 1080p video transmission. The operating speed is about 270Mbps which outperforms the required speed of 148Mbps. The HDMI interface designed is verified on the test board with Vertex 6 FPGA.

Keywords—HDMI, TDM S, LCD Controller, 3D TV.

I. INTRODUCTION

HDMI (High Definition Multimedia Interface) [1] is suitable for 3D video transmit. HDMI is a compact audio/video interface for transferring uncompressed video data and compressed/uncompressed digital audio data from a HDMI compliant device to a compatible computer monitor, video projector, digital television, or digital audio device.

Fig. 1 illustrates the structure of HDMI interface designed. LCD controller fetches stereo 3D video [2] from memory and sends the data to HDMI source module through RGB interface. Then, HDMI source transmits the data to HDMI sink through TMDS(Transition Minimized Differential Signaling) channels. After HDMI sink receives video image [3], the stereo display controller distributes the video data to two display devices[4].

Fig. 1 High-speed Video Transmission Interface

Fig. 2 LCD Controller block diagram

II. HDMI AND LCD CONTROLLER

A. LCD Controller

LCD controller provides video data from frame memory and generates correct timing for video synchronization signals[5]. The LCD controller is illustrated in Fig 2. Master interface is a DMA(Direct Memory Access) which fetches frame data from memory. Slave interface has registers that are used to program video synchronization timings. The FIFO and Timegen modules are used to provide data at the required timing.

Fig. 3 Timing diagram

B. HDMI Structures

HDMI can transmit video, audio and auxiliary data through TMDS channels that consists of one clock and three data pairs as shown[6] in Fig 4. The TMDS performs 8-bit to 10-bit encoding to minimize transition and balance the DC component.
The received data in the HDMI sink is decoded to provide the original video data[7].

![HDMI structures](image1)

**Fig. 4 HDMI structures**

**C. HDMI Source**

As shown in Fig. 5, the HDMI source receives external video data and adds a packet header for a format suitable for a specific display. Video data is encoded to a 10-bit format for DC balance to minimize 1/0 transitions. This will maintain stable DC performance despite changes in temperature, power supply voltage, and operating mode[2]. After the encoding, the data is packetized and serialized for the transmission in TX PHY.

![Block diagram of HDMI Source](image2)

**Fig. 5 Block diagram of HDMI Source**

**D. HDMI Sink**

Three TMDS video data and one TMDS clock channels are used for transmission through the HDMI cable. As shown in Fig. 6, the HDMI sink receives the data from RX PHY and the data is parallelized and decoded for transmission to video interface.

![Block diagram of HDMI Sink](image3)

**Fig. 6 Block diagram of HDMI Sink**

**III. MODELSIM SIMULATION**

**A. LCD Controller**

The 8-bit color data are entered as vdin signals. vdin is encoded to 10-bit encoded signal v_out as shown in Fig. 8. The transmission will start after a guard band for marking the beginning of the video period.

![Encoder](image4)

**Fig. 8 Encoder**

The 8-bit color data are entered as vdin signals. vdin is encoded to 10-bit encoded signal v_out as shown in Fig. 8. The transmission will start after a guard band for marking the beginning of the video period.

![Serialization](image5)

**Fig. 9 Serialization**

Fig. 9 shows a serialization process. The encoded 10-bit signals are serialized to 1-bit signal edin and edin is transmitted at every serial clock.
C. TMDS Sink

In Fig. 10, clock is recovered and data is parallelized to convert to 10-bit data at TMDS Source. Because it is transmitted from LSB, after shifting to the right, it will be sent when it becomes 10-bit.

IV. RESULTS
The design is verified in Modelsim and validated in FPGA implementation. Table I shows the synthesis results. The target operating speed is 148M bps and the achieved speed is 271M bps. Therefore, this design can be used for stereo 1080p video device. For the FPGA implementation, we used Xilinx Vertex 6 and synthesized with ISE.

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REFERENCES