Analysising the Effect of Heat on Layers of a Printed Circuit Board

Tawanda Mushiri, and Charles Mbohwa

Abstract—As is well known, designers are fast approaching ever more performance out of printed circuit boards. Power densities are on the rise, and so are high temperatures that can wreak havoc on conductors and dielectrics. Elevated temperatures - whether from power losses or environmental factors - affect thermal and electrical impedances, causing erratic system performance, if not outright failure. Differences in thermal expansion rates – a measure of the tendency of a material to expand when heated and shrink when cooled – between conductors and dielectrics generate mechanical stresses that cause cracking and connection failures, especially if the boards are subject to cyclic heating and cooling. If the temperature is high enough, the dielectric can lose its structural integrity altogether, knocking over the first domino in a cascade of trouble. Of course, heat-generation has always been a factor in PCB performance, and designers are accustomed to including heat sinks into their PCBs, but the demands of today’s high power-density designs frequently overwhelm traditional PCB heat-management practices. Mitigating the effects of high temperatures has far-reaching implications, not just for the performance and reliability of PCBs, but also for such factors as: Component (or system) weight, Application size, Cost and Power requirements.

In this article we will discuss some design methods and PCB technologies used in fabrication and PCB assembly to help the designer cope with high-temperature applications. A FEM will be used to test and analyse the thermal effects of heat on PCBs.

Keywords—Printed Circuit Board, Thermal resistance, Finite element analysis.

I. INTRODUCTION

Printed circuit board is a conglomeration of organic and inorganic materials with external and internal wiring, which allows electronic components to be physically integrated, and electrically connected (T. Hatakeyama et al, 2011). Over the past several decades, printed circuit board technology has developed substantially. Early printed circuits were fabricated by printing a pattern of polymer resist on a copper plane and then chemically etching. Holes drilled in the laminate held the component leads that were soldered to the copper-printed patterns. The technology has progressed in developing the sophistication and uses of the printed circuit board interconnections. Today, the basic functions of the printed circuit board are the same: the interconnecting copper signal lines join two I/O leads from two different components. The components may be resistors, inductors, capacitors, or semiconductor chips. When applying multichip technologies, there may be hundreds of components attached to the printed circuit board. The ever-increasing level of complexity of printed circuit boards has forced primitive boards using a few yards of printed wiring in the 1960s, to evolve into sophisticated, multi-layered structures requiring kilometers of printed wiring (W. Nakayama et al, 2008). This increase in the circuit board level of sophistication can be attributed to the integration of semiconductors and an increased need for I/O capabilities. The most complex printed circuit boards contain kilometers of copper interconnection, roughly 50 to 100 microns wide, and half as thick. These boards distribute KW/m^2 of power internally in very densely packed layers of copper. The drive for higher performance means that there is a greater requirement for power-handling and cooling capabilities. It is the responsibility of the designers to ensure that cooling on the printed circuit board is adequate under all possible load conditions in order to allow proper performance of the individual components and the board as a whole. Therefore, it is imperative that the designers understand and are able to predict the temperature distribution on multilayered structures prior to prototype production. The overriding reasons for performing a precise thermal analysis are to increase component reliability, ensure proper material selection, reduce the possibility of catastrophic thermal failure, and guarantee electrical performance. Designing a cost competitive power electronics system requires careful consideration of the thermal domain as well as the electrical domain. Over designing the system adds unnecessary cost and weight; under designing the system may lead to overheating and even system failure. Finding an optimized solution requires a good understanding of how to predict the operating temperatures of the system’s power components and how the heat generated by those components affects neighbouring devices, such as capacitors and microcontrollers. No single thermal analysis tool or technique works best in all situations. Good thermal assessments require a combination of analytical calculations using thermal specifications, empirical analysis and thermal modeling. The art of thermal analysis involves using all available tools to support each other and validate their conclusions.

This paper first presents the basic principles of thermal systems and then describes some of the techniques and tools.
needed to complete thermal effect of heat analysis. Printed circuit boards are the primary focus.

A. Problem Statement

Every non-ideal electrical component conducting a current is a potential heat source, due to the fact that they include an electric resistance which converts the kinetic energy of electrons (current) into heat energy. This process is often referred to as Joule heating. Due to ever decreasing sizes of components and more advanced production technologies the general trend in PCBs is to arrange more and more components in small areas. This entails a higher concentration of heat sources on the board and thus enlarges the significance of heat management considerations. Too high temperatures pose a threat to sensitive components such as chips and processors but can also affect adjacent structures and thus the functionality of the whole system. Thus the general goal is to design a well-defined heat transfer from these sources into safe regions of lower temperature (sink).

B. Aim

The main aim of this project is to demonstrate the finite element analysis on the thermal effect of heat on layers of a printed circuit board.

C. Objectives

The main objectives of this study are:

- To investigate the effect of heat on layers of a printed circuit board.
- To reduce risk of multiple board re-spins due to thermal problems
- To understand the thermal behavior of PCB designs with LISA softwares.

II. Scope Of The Study

The present investigation of the thermal analysis of the effect of heat on PCB using FEA was started with the intent to investigate the relative importance of several factors in the nonlinear finite element analysis of PCB material. These include the effect of the size of the finite element mesh on the analytical results and the effect of the nonlinear behaviour of thermal conductivity of components on the PCB. In the progress of this study improved material models were developed and included in the analysis.

III. Justification

A. Reliability

Reliability is defined as the probability that a component is functioning as designed, while failure is defined as the probability that a component is not functioning as designed. There is a predictable relationship between the operating temperature of electronic components and reliability. The materials used in the fabrication of these components have thermal limitations, and should these thermal limitations be exceeded, the physical and chemical properties of the material are affected, and the device fails. Failures at short times are called early fails, or infant mortality, while failures at long times are called wear out fails because they result from usage. At all times, failures can occur from intrinsic mechanisms, or from random overstress. Provided the device has been adequately designed, early failures can arise as a result of manufacturing defects. Defects that occur early on, or the "burn-in" period, are considered to be the result of poor or inadequate quality control mechanisms in the manufacturing process, therefore the need for a proper thermal analysis before manufacturing.

B. Material

The fabrication of printed circuit boards results in the joining of different materials. The materials selected can have a significant impact in thermal properties of the printed circuit board. In the largest circuit boards hundreds of amps may be switched at once. As packaging densities increase thermal, mechanical, electrical, and chemical coupling becomes very strong. In view of the complexity of electrical structures today, computer modeling of total thermal response of a printed circuit board is a requirement conducive to understanding one of many interactions.

C. Thermal Fatigue And Catastrophic Thermal Failure

Printed circuit boards are comprised of dissimilar materials that expand at different rates of heating. The differential expansion of mismatch must be accommodated by the various elements on the board. The increasing levels of packaging densities and board complexity dictate the need for designing a thermal environment that can accommodate the diverse components that are in close proximity to each other. As previously mentioned it is very important that the board designers have an understanding of the operating environment in which the board will be operating in order to incorporate into the design the tolerances that will allow the product to operate reliably. Catastrophic thermal failure is defined as an immediate, thermally induced, total loss of electronic function in a specified component. This type of failure comes as a result of excessive temperature, or a thermal fracture. Catastrophic failure comes about as a result of many factors including the operating environment, equipment history, mechanical loading, and operational modes of the component. Although it is difficult to predict the temperature at which thermal failure may occur, it is possible to establish with the aid of thermal analysis the boundaries at which the board can be expected to operate reliably and within its useful operating life cycle.

IV. Literature Survey

Printed circuit board (PCB), which is also referred as printed wiring board (PWB), is used primarily to create a connection between components, such as resistors, integrated circuits, and connectors. It becomes an electrical circuit when components are attached and soldered to it, which then is called printed circuit board assembly (Figure 1).
V. METHODOLOGY

In this research project FEA is going to be done were the objects to be modeled are divided into many smaller pieces, called “elements,” within which the complex heat transfer processes are approximated by simpler algebraic equations involving the temperatures at a finite number of points called “nodes”. The list of available element types includes three-dimensional (3D) “solid” elements, such as hexahedrons (bricks), tetrahedrons, and wedges; two-dimensional (2D) “plate” elements, such as triangles and quadrilaterals; and one-dimensional “resistor” elements.

The simplest approach to modeling heat conduction within a PCB would be to create an extremely fine mesh of solid elements that incorporates every detail in three-dimensions, no matter how small. This approach is considered completely unfeasible because the model size would be prohibitively large for typical PCBs. Today’s multi-layer boards can have as many as 50 layers and thousands of complex traces.

The finite element model described here makes use of realistic approximations to incorporate the important heat conduction details, yet keep the model size feasible for rapid solution on the latest generation of PCs. First, the thermal conductivity of the copper trace layers is high enough that the temperature gradient through these thin layers can be neglected. This allows a two-dimensional mesh of elements to represent the in-plane heat conduction for a typical trace layer containing thin line traces and or larger solid copper areas. In the present application, an unstructured triangular mesh is used to accommodate the complex geometrical features of the PCB and the outlines of the attached components, enabling accurate modeling of the PCB boundary conditions and the component connections. Each dielectric layer in the PCB is modeled by a single layer of wedge-shaped solid elements, enabling heat conduction between the copper (trace) layers to be modeled accurately. An efficient and automatic mesh generation procedure based upon extruding an initial 2D mesh of triangles is employed here to obtain the layers of nodes and elements.

In order to keep the model size reasonable, the triangular mesh does not explicitly represent the polygonal boundaries of the individual traces. Instead, each triangular plate region is given effective anisotropic conductivity properties, computed to represent the line traces and solid copper regions within its boundary. The finite element model is actually created by converting these plate elements directly into a triangular network of resistor elements, each given its own unique and appropriate resistance. This is much simpler than creating many thousands of plate elements, each having unique anisotropic material properties, and the thermal conductivity of these traces is still accurately accounted for. With a reasonably fine initial 2D mesh of triangles, the complex temperature distributions in the PCB are well represented, and the component temperatures are computed accurately. For complex boards with many layers and hundreds of traces, it is not unusual to obtain 2D meshes containing 5,000 or more triangles.

Computation of the resistor network representing a filled trace is done as follows. First, for each triangle that is completely within the trace boundary, the triangle is converted into three thermal resistors that exactly represent the thermal conductivity of the corresponding solid copper triangular plate. For triangles that are only partially inside the trace boundary, the three resistors are computed as above, but the resistance values are then adjusted (increased) to account for the reduced conducting area, and resistors are omitted where the conduction path is interrupted.

Computation of the resistor network representing a line trace is done as follows. The centerline of the trace is described by a set of straight-line segments, each of which overlaps one or more triangles along its path. For each overlap, the portion of the straight-line segment that overlaps is converted into a thermal conductor, which is then transformed into a set of three equivalent thermal resistors aligned with the triangle edges and connected to nodes at the corners.

Automatic construction of the initial 2D mesh of triangles is performed in a three-step procedure. First, an appropriate set of straight-line segments representing the boundaries of important geometrical details is created. Second, the geometry is cleaned up by removing segment intersections and by organizing the straight-line boundary segments into closed loops and regions. Finally, a set of nicely shaped triangles (with no small interior angles) is created using a numerical procedure named deLaunay mesh generation, which is well known in the computational geometry literature.

The 3D finite element PCB model is obtained from the initial 2D triangle mesh through the following “extrusion” process. First, the nodes in the 2D triangle mesh are copied onto many planes at the appropriate positions through the PCB thickness. These nodes are then connected to the wedge-shaped solid elements representing the dielectric layers. Next, the planar resistor networks representing the conducting layers are connected to these nodes. Finally, the resistors representing vias are added. In the typical situation where
conducting layers alternate with dielectric layers, each plane of nodes connects to resistors representing a conducting layer, plus the solid elements representing dielectric layers above and/or below the conducting layer.

Thermal vias connecting trace layers are modeled by adding effective resistor elements connecting between the corresponding layers of nodes in the copper trace layers. Similar to the methodology used in representing individual traces, resistor elements are added at the specific meshed element where the via resides to enhance the local heat transfer through the board.

VI. HEAT TRANSFER

The degradation of the heat flow capabilities of a printed circuit board can lead to reliability problems due to excessive operating temperatures. It is imperative that designers incorporate into the board the capability to maintain temperatures within upper operational limits while operating in all possible environments in which the board will be exposed. Heat transfer is defined as all energy flows that arise as a result of temperature differences. Because the components mounted on printed circuit boards and, indeed, the printed circuit boards themselves are not one hundred percent efficient, heat is generated. The primary modes of heat transfer are conduction and convection. Conductive modes include mechanical thermal contact and solid thermal interfaces between materials, such as copper, solder, or epoxy layers. Convective modes include natural and air forced cooling, and forced liquid cooling. Radiation is also a factor; however, it is not as significant as conduction and convection at the temperatures in which printed circuit boards operate

VII. RESULTS AND SIMULATIONS

Figures 2 illustrate a typical conducting layer with many filled and unfilled traces and its finite element equivalent resistor network. Note that many traces can overlap an individual triangle. Clearly, many more elements would be necessary to represent the interior of each line trace explicitly by plate elements, and each trace outline would have to be constructed based upon the line width and centerline.

Fig 3 Simulated results of a PCB.

VIII. RECOMMENDATIONS AND CONCLUSION

This article has described some efficient steps to follow for accurately modelling the conduction of heat within the layers of a printed circuit board using finite element analysis. This procedure is based upon separate representations of the dielectric and conducting layers. A key feature is the use of an equivalent resistor network to represent the traces in a conducting layer and vias between layers. In this manner, the size of the finite element model is kept manageable, while key details are preserved for an accurate solution.

REFERENCES
