PWM Based Closed Loop Control of Soft Switched Non Isolated High Multiplying Factor DC-DC Boost Converter

Sreeja.P and Dr.L.Padma Suresh

Abstract— There is an ever growing demand for high step up DC-DC converters with power conditioning due to large and sudden fluctuations in load such as DC drives. Such DC-DC converters should boost voltage as low as 20-30V to 400V and regulate the output voltage during sudden load transients. When switched at very high frequency to meet dynamic & steady state requirements, the losses add on in the converter. Switching on at zero voltage and Switching off the switches when current through them is zero is one possible solution to minimize the switching losses which can be achieved with the help of resonating circuit. One should have tradeoff between high switching frequency and switching losses. With an optimum design of circuit parameters and resonating elements, high step up voltage can be obtained. One such approach where an input DC voltage of 70V is boosted to 554.5V with Zero Voltage and Zero Current Switching (ZVZCS), with reduced switching frequency compared to all existing configurations is presented in this paper. A Pulse Width Modulated (PWM) closed loop control is employed to this converter to enhance the load regulation and reliability of the converter. The closed loop control scheme and simulation results are presented in this paper.

Keyword--- PWM Control, PI controller, High Gain DC chopper, Parameter Optimization, Non-isolated, Soft switched, Closed loop Control.

I. INTRODUCTION

The demand for non-isolated high step-up dc–dc converters has been gradually increasing in accordance [1] with the growth in dc backup energy systems for uninterruptible power system (UPS). There are two major concerns related to the efficiency of a high step up dc–dc converter: large input current and high output voltage [3-9].

The large input current results from low input voltage; therefore, low voltage rated devices with low on state resistance are necessary in order to reduce the conduction loss. The boost and buck-boost converters are the simplest non-isolated topologies. The non-isolated converters can provide high step-up voltage gain without incurring extreme duty ratios. Shih-Kuen Changchien and Tsorng-Juu Liang [2] in 2003 proposed a novel high step-up dc–dc converter, which utilizes a voltage doubler and adjusts the turn ratios of the coupled inductor. This converter has been highly efficient because it recycles the energy stored in the leakage inductor of the coupled inductor, but stress across the switches is high and large inductor leakage current may damage the switches. Transformerless DC–DC Converters with High Step-up voltage, was developed by Gain Lung-Sheng Yang, Tsorng-Juu Liang [11] in 2009. This converter uses two inductors with the same level of inductance are charged in parallel during the switch-on period and are discharged in series during the switch-off period. However this converter uses only one active switch for the energy conversion, which also suffers very high current during the switch-on period. The converter is suitable for low-to-middle-power applications. Yi-Ping Hsieh and Jiann Fuh Chen in 2011 proposed a novel, high efficiency, and high step up dc–dc converter [12]. By using the capacitor charged in parallel and discharged in a series by the coupled inductor, high step-up voltage gain and high efficiency are achieved. This converter experiences extremely high input current at full load, which would lead to high conduction loss during the switch turn-on period. Another ZVZCS based topology was proposed by Yohan Park, Byoungkil Jung, and Sewan Choi in 2012 [9].

This converter shows zero-voltage switching turn-on of the switches in continuous conduction mode as well as reduced turnoff switching losses owing to the switching method that utilizes \( L_r - C_r \) resonance in the auxiliary circuit. Also, as a result of the proposed switching method, the switching losses associated with diode reverse recovery become negligible even in the small duty cycle. The capacitance in the auxiliary circuit is significantly reduced compared to the pulse width modulation method. ZCS turnoff if main switches is not attained in this topology. A high step up DC-DC converter with optimized parameters is designed which yields better output voltage compared to the converter in [12] with reduced switching frequency and the switching losses. The closed loop control to regulate the output voltage is introduced which is
based on PWM based control. The load is increased by 10% of its rated value, which can be the maximum allowable change under stringent condition. The simulation results for optimized design of ZVZCS switched non isolated dc-dc boost converter with high voltage gain for open loop were given by the same authors[13]. The corresponding simulation results are presented in this paper.

II. CONVERTER OPERATION

Figure 1 shows the converter topology which has the same topology proposed in [12], but with different design specification. The converter consists of a general boost converter as the main circuit and an auxiliary circuit which includes capacitor $C_r$, inductor $L_r$, and two diodes D1 and D2. Two switches S1 and S2 are operated with asymmetrical complementary switching to regulate the output voltage.

![Fig. 1 High Voltage gain DC-DC boost converter](image)

Owing to the auxiliary circuit, not only output voltage is raised but ZVS turn-on of two switches can naturally be achieved in continuous conduction mode by using energy stored in filter inductor $L_f$ and auxiliary inductor $L_r$. Unlike PWM method in which the switches are turned OFF with high peak current, the proposed converter utilizes $L_r-C_r$ resonance of auxiliary circuit, thereby reducing the turn-off current of switches. Furthermore, for resonance operation, the capacitance of $C_r$ is reduced by a greater value. Various modes of operation are shown in Figure 2.

![Fig. 2. Modes of operation](image)

III. DESIGN SPECIFICATIONS

Design of $f_r$

The resonant frequency $f_r$ is determined by

$$f_r = \frac{1}{2\pi \sqrt{C_r L_r}}$$

Below resonance $2f_r > \frac{f_s}{D_{eff}}$ and above resonance $2f_r < \frac{f_s}{D_{eff}}$

Where $f_s$ is switching frequency and $D_{eff}$ is effective duty ratio $= D-\Delta D$ (2)

D is duty ratio.

Design of Filter Inductance Considering the input current ripple $\Delta I_{in}$, input filter inductor $L_f$ is determined by

$$L_f = \frac{1}{2} \frac{DV_{in}}{\Delta I_{in} f_s}$$

$\Delta I_{in}$ = 20% and $\Delta V_0$ = 5%

Design of $C_r$ and $L_r$

In order to satisfy the ZVZCS condition $L_r$ is determined using the equation

$$\frac{1}{2} L_r (I_{Lr+pk} - I_{Lr min})^2 = \frac{1}{2} (C_{os1} + C_{os2}) \left( \frac{V_i}{1-D} \right)^2$$

Where $C_{os1}$ and $C_{os2}$ are the output capacitances of switches S1 and S2 respectively.

Once $L_r$ is fixed, $C_r$ is found by using equation (1)

The designed values are listed in Table I.
IV. SIMULATION RESULTS

The open loop simulation is carried out for an input supply voltage of 70V, which shown in Figure 3. Figure 4.(a) and (b) shows Switching pulse of S1, voltage across S1 and Current through S1. Figure 5 shows Switching pulse of S2, voltage across S2 and Current through S2.

As observed from Figures 4 and 5, during the rise time of both the switches, the voltage across them is zero, which ensures ZVS turn on of both the switches. During the fall time of switches, the currents IS1 and IS2 are decayed to zero which implies ZCS turn off of both the switches. Hence ZVS turn on and ZCS turn off of all switches is achieved. As observed from the above simulation results, VS1 and VS2 are equal to 10V. Therefore the stress across the switches during non-conduction period is very much lesser compared to the earlier configurations.

Figure 6 shows resonating capacitor and inductor voltages. At resonance both Cr and Lr voltages are equal and that voltage appears across switch during their turn off state. Figure 7 shows the load voltage. Which is 554.5V which is 1.5 times greater than the proposed design in [12]. Hence high step up is achieved with the current design. The output Current is shown in Figure 8. Since both the output voltage and currents are high, this design gives high step up and high output power compared to existing designs and topologies.

The comparison of various parameters is listed in Table 1.
A load disturbance is introduced. Load change of 10% of rated load is introduced at 0.002 sec and the corresponding load voltage with this additional load is shown in Figure 8.

It is evident from Figure 8 that when the load resistance increased by 10% of rated load, the voltage is decreases and attains a steady value of 326.7V at 0.006 sec. Therefore for 10% rise in load, the voltage is decreased by 40% which is not desirable for the critical loads. Hence a closed loop control scheme is adapted. The simulation circuit for the closed loop control is shown in Figure 9. The output voltage is sensed and compared with the reference voltage of 554.5V. The error signal is given to a PI controller whose initial settings are listed in Table 1. The output of a PI controller is given to an inverting op-amp comparator. A carrier signal of 25kHz is applied to the non-inverting terminal of comparator. The output of op-amp comparator is a PWM signal which is given as gate pulse to main switch S1. Complement of this PWM output is given as trigger pulse to switch S2. The respective output voltage and currents are shown in Figure 10 and 11 respectively.

As observed from Figure 10, when the load is increased by 10%, the output voltage momentarily, but due to closed loop control it it follows the reference voltage which is taken same as the output voltage during normal operating condition. The output voltage is 553.8 V which attains a steady value at 0.00346secs. When the load increases as observed from Figure 11, the current increases, but due to PWM control, it comes back to the original value. Therefore output power balance is maintained.

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**TABLE I**

Comparision of Performance of the Proposed Design and RPWM Method in [12]

<table>
<thead>
<tr>
<th>Component/Value</th>
<th>RPWM Method</th>
<th>Proposed Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage (V)</td>
<td>70V</td>
<td>70V</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>50kHz</td>
<td>25kHz</td>
</tr>
<tr>
<td>Filter Inductance</td>
<td>50 µH</td>
<td>50 µH</td>
</tr>
<tr>
<td>Resonant Inductor L&lt;sub&gt;r&lt;/sub&gt;</td>
<td>6 µH</td>
<td>8 µH</td>
</tr>
<tr>
<td>Resonant Capacitor C&lt;sub&gt;r&lt;/sub&gt;</td>
<td>2.7 µF</td>
<td>2.6 µF</td>
</tr>
<tr>
<td>Load Resistance</td>
<td>70Ω</td>
<td>70Ω</td>
</tr>
<tr>
<td>Output Capacitor</td>
<td>30 µF/250V</td>
<td>10 µF/70V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>380V</td>
<td>542V</td>
</tr>
<tr>
<td>Initial PI gain constant</td>
<td>-</td>
<td>0.33</td>
</tr>
<tr>
<td>Controller time constant</td>
<td>-</td>
<td>0.096sec</td>
</tr>
</tbody>
</table>

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Fig. 7 Output Voltage (554.5V) during normal operating condition

Fig. 8. Output voltage during the increase of load resistance by 10%
V. CONCLUSION

A DC-DC converter for high step up and high power applications is proposed. From the simulation results it is observed that ZVS turn on and ZCS turn off of all the switches is obtained. The voltage stress across the switches is much lesser. From the comparison of results with the existing design it is observed that the Capacitor size and inductor volumes are reduced in the proposed topology by adapting proper switching scheme. The switching frequency is also less which is an indication for reduced switching losses. A PWM based closed loop control ensures voltage regulation during load change. From simulation results it is brought in to notice that during load change, though output voltage follows the reference voltage, there are ripples in the output voltage and current. Hence the work can be extended to minimize the ripple by using an additional hysteresis current controller or an artificial intelligent controller, since pulsating voltage and current produce pulsating torque if this converter is used for DC drive application.

REFERENCES


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