Comparing Single and Three-stage Structures of the Decimation Filter used in ADSL

H. Fathabadi

Abstract — This paper describes two structures of the digital decimation filter which is used in $\Sigma \Delta A/D$ converters in ADSL. Single FIR and three stages comb-FIR-FIR the two presented structures. The hardware minimization is considered for each structure and the final simulation results and implementations are presented. Finally, a comparison between the two structures is done to choose the best structure based on the hardware cost.

Keywords — ADSL, comb filter, decimation filter.

I. INTRODUCTION

ASYMMETRICAL Digital Subscriber Line (ADSL) is an application of the digital signal processing techniques which enables home users and consumers to access the high speed applications of internet such as video-on-demand. ADSL provides a downstream capability up to 4 Mbit/s over the existing telephone wires, within a distance up to a few kilometers. Analog signal transmission of ADSL requires high speed and high resolution Analog-to-digital (A/D) converters. A/D converters can be implemented using $\Sigma \Delta$ modulators which allow high sampling rate meanwhile minimize the hardware [1], [2], [3]. High resolution can be achieved through filtering and decimating a high rate bit stream [4].

II. ADSL STRUCTURE

Fig. 1 shows a schematic diagram of the ADSL. Data conversion in ADSL requires 12 bits of resolution at 4 MHz [5]. The decimation filter highlighted in Fig. 1 is used for reducing the sampling rate from 64 MHz to 4 MHz and also achieving the appropriate resolution which is necessary. The specifications of the decimation filter are shown in Table 1.

III. SINGLE STAGE MULTI RATE FIR FILTER

A single stage realization of the decimation filter can be done using a multi rate FIR filter. The frequency response and unit step response of the proposed single stage multi rate FIR decimation filter are shown in Fig. 2 and Fig. 3, respectively. The order of the proposed FIR filter is 152, so the filter requires many numbers of coefficients (153 coefficients). The implementation of the proposed single stage FIR decimation filter can be done by choosing one of the following methods:

1) A RAM is used to store the input samples and a ROM is used to store the coefficients.

2) Reduction in hardware complexity and power consumption can be done using signed digit (SD) representation. SD representation of A is as the form of $A = \sum_{k=-M}^{N} a_k 2^k$ where $a_k \in \{-1,0,1\}$, M and N are positive integer number. The minimal SD representation uses only two non-zero digits, for example minimal SD representation of 0.484375 is $6 -12 -2^2$, so only two right shifts of the input sample and only one “ADD” are required to perform the multiplication. As a result, the implementation of the filter is done using only some shift registers (instead of the RAM and the ROM mentioned in the first method).

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In fact, minimal SD representation of the coefficients allows that the implementation of the normalized coefficients \( |C_k| \leq 1 \) can be done with only right shifters subsequently wasting area and power is effectively reduced [5], [6], [7]. Based on the method 2 and by exploiting the symmetry of filter coefficients, the implementation of the proposed single stage multi rate FIR decimation filter can be done using 307 right shift registers (153 right shift registers are used to store input samples and 154 right shift registers are used for filter coefficients according to the SD representation.

IV. MULTISTAGE ARCHITECTURE OF THE DECIMATION FILTER

Single stage FIR, which was presented in section 3, require so many coefficients that results to occupy a large area of the silicon chip. To solve this problem a multistage architecture is a good solution. It is clear that an anti-aliasing filter is necessary in order to reduce the sampling rate. An appropriate multistage architecture is comb-FIR-FIR that consists of the following stages:

- A pre-filter with the comb behavior and subsequently a frequency response as the form of
  \[ H(z) = \sum_{n=0}^{N-1} z^{-n} \]  

- A FIR equalizer to compensate the attenuation in the band pass region done by the pre-filter.

- A FIR filter as third stage with very steep transition behavior for making a suitable stop-band attenuation.

Sampling rate in the input of the two architectures (64 MHz) can be reduced with the factor of \( 2^n \) in the first and other stages. This results the factorization of the decimation factor and subsequently reducing the very huge computation tasks. In the proposed decimation filter, the sampling frequencies in the first, the second and the third stage are chosen as 16 MHz, 8 MHz and 4 MHz, respectively. It is clear that sub-sampling factors for the first, the second and the last stage are 4, 2 and 2, respectively.

V. IMPLEMENTATION OF THREE-STAGE COMB-FIR-FIR FILTER

In this section the implementations of the three-stage comb-FIR-FIR decimation filter is presented. The block diagram of the filter is shown in Fig. 4 and the number of the right shift registers needed for implementation of each stage of the proposed filter is separately presented. The order of the FIR equalizer filter is 46, consequently the implementation is done using only 95 right shift registers. Also the last stage of the decimation filter is a FIR filter which is implemented using only shift registers because of using minimal SD representation of the coefficients. This FIR filter improves the transition response of the final decimation filter. The order of this filter is 86, so it can be implemented using 175 right shift registers. The frequency response of the whole comb-FIR-FIR decimation filter is shown in Fig. 5.

VI. A COMPARISON BETWEEN FOUR PROPOSED STRUCTURES

Two structures of the digital decimation filter used in ADSL were presented in previous sections. Based on the minimal SD representation of the coefficients, a comparison between the two structures is done in Table 2. The comparison shows that the three-stage comb-FIR-FIR decimation filter requires the hardware which is less than the single stage multi rate FIR filter.
TABLE II
A COMPARISON BETWEEN FOUR PROPOSED STRUCTURES

<table>
<thead>
<tr>
<th>Structure</th>
<th>Number of Right Shift Registers Used in Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi rate FIR decimation filter</td>
<td>307</td>
</tr>
<tr>
<td>Three-stage comb-FIR-FIR decimation filter</td>
<td>95+175=270</td>
</tr>
</tbody>
</table>

VII. CONCLUSION

In this paper, two structures of the digital decimation filter used in $\Sigma \Delta A/D$ converters of ADSL were presented. These two structures were single multi rate FIR and three-stage comb-FIR-FIR. The hardware minimization was done using the minimal SD representation of the coefficients for each filter. A comparison between the two structures was done to choose the best structure which has minimal hardware.

REFERENCES


