DC Link Capacitors Voltage Balancing in Diode-Clamped Multilevel Inverter

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Abstract—In all multilevel topology with several DC link, the voltage balancing problem of DC capacitors is a key problem. This paper proposes a new topology of chopper circuit for dc capacitor voltage balancing in diode clamped multilevel inverters (DCMLI). In the presented topology the number of switches is reduced respect to other proposed topology in literatures. Suggested topology is modular and has high reliability. Based on presented control system for chopper switches, only one switch is turn on at each time. Therefore the conduction and switching losses of chopper system are reduced. The presented simulation results show fast dynamic response of suggested chopper and reduction the voltage stress on its switches. Computer aided simulations are performed through MATLAB/Simulink software. The simulations results are presented to verify the performance of proposed chopper circuit and its control system for DC capacitor voltage balancing in diode clamped multilevel inverter.

Keywords— Chopper, Capacitor voltage balancing, Diode clamped inverter, H-bridge.

I. INTRODUCTION

In recent years, multilevel inverters have presented an important development to reach high power with increasing voltage levels. The multilevel converter present great advantage compared with conventional two level converters such as; high power quality of wave forms, low switching losses, high voltage capability, low electromagnetic compatibility (EMC), etc [1, 2]. Multilevel converters can be divided into diode clamped multilevel converter (DCMC), flying capacitor multilevel converter (FCMC), and cascaded multilevel converter (CMC) with separate DC sources [3, 4].

Recently, attention has been paid to multilevel inverters for medium-voltage and high-power applications such as STATCOM, SSSC, UPFC, high voltage direct current transmission as well as SVC applications, etc. [5, 6]. The DCMC some features as below:

1- The dc capacitors can be easily pre-charged
2- The control of switches is very simple.
3- The protection of this inverter circuit is less complex than other inverter [8-9].

The above mentioned features are obtained when the voltage divisions on the capacitors under different working conditions are equal. Non-uniform voltage on the capacitors can be reduced the quality of inverter output voltage [7]. Main problem of DCMC is unbalanced charging of capacitors in different operating points. The following methods are used to overcome the unbalanced charging of capacitors voltage:

1- Reform and changing the switching pattern and controlling of switches [3-10].
2 - Installation of capacitor voltage balancing circuits on the DC side of the inverter.

The first solution is preferable in terms of cost and reduces the complexity of system and additional circuits and increases the flexibility of the circuit.

Increasing switching frequency in conventional choppers causes to reduction of output ripple, size and weight of circuit. But Increasing switching frequency has some problem such as:

1- High stress on switches [7].
2- Increasing the Electromagnetic interference (EMI) [1-4].
3- Increasing the switching losses [7].

In this paper a novel chopper circuit is proposed to overcome the voltage unbalance problems in capacitors of a DCMC. In comparison with conventional choppers, it requires less number of switches. Also, switching frequency and stress on the switches are reduced and all mentioned problems are solved without increasing the circuit size and weight.

Simulation results carried out by MATLAB/Simulink in different operating conditions are presented to verify and validate features of presented topology.

II.PROCEDURE FOR PAPER SUBMISSION

A single phase of five levels DCMC is considered here and its circuit is shown in Fig.1(a). Fig.1(b)and1(c)show conventional chopper and three level flying capacitor based chopper circuit for capacitor voltage balancing, respectively. Fig.1(b) the inverter side DC link includes capacitors C1-C4 which the voltage of each capacitor must be equal to \( V_{dc} / 4 \). With considering the point n as neutral reference, the inverter output voltages can be expressed as Table 1[7, 8].

In the Table 1, state 1 means switch is on and state 0 means switch is off. When currents i2 and i4 have a non-zero average value, DC link Capacitors of DCMC will be suffer imbalanced voltage [9-10]. To avoid this phenomenon, the presented chopper circuits in Fig.1 (b) and 1 (c) are discussed in [7].

Both chopper in Fig.1 (b) and 1 (c) consist two separate...
parts. It should be noted that the resistances R1 and R2 in Fig.1 (b) represent the resistance of the corresponding inductors and capacitors Cf1, Cf2 in Fig.1(c) are called suspension capacitance that these suspension capacitances are keeping the voltage stress of switches on $V_{dc}/4$.

In this paper a novel chopper circuit based on parallel switches for capacitors voltage balancing is presented. The presented chopper can be used in DCMC and is shown in Fig. 2. The proposed new multi-level chopper has the benefits of conventional and flying capacitor choppers that were described in the previous section. Also, it can partially overcome to the problems of previous mentioned choppers.

### III. PROPOSED CHOPPER CIRCUIT

#### A. Performance of proposed chopper in different modes

The main objective of proposed chopper is capacitors charging. Fig. 3 shows the paths of current flow in different modes. According to Fig. 3, the first charging priority is with capacitor C1 and then C2, C3 and C4 are charged, respectively.

With these priorities as circuit strain function when every capacitor charging in himself lawful band and it capacitor via switch in the parallel branches issue the certain path (For example, capacitor C1 switches S2) and the next capacitor starts to charge up, and this procedure until all the capacitors in Range considered to be charged, it will continue.

Assume ago startup the circuit all of the capacitor consist of zero primary voltage and all of the switch are no connected, then in the $T = 0$ (at start-up circuit), switch $S_1$ is connected since $V_{c1}$ is zero ($V_{c1}=0$), with connecting the switch $S_1$ the capacitor $C_1$ to be charged to the capacitor $C_2$ and the same procedure will continue up until the next capacitors are charged ($C_3$-$C_4$).

Because all diodes in this circuit are directly Bias (D1-D4), so if C1 or any of the capacitors have extra energy can be this extra charge through the diodes transfer to the next capacitors. It should be noted that the resistors $R_1 = R_2 = R_3 = R_4$ in Fig4 (a) represent the winding resistance of corresponding inductors L1-L4.

With note the up detail in each section of circuit function alone one switch is on, only when C4 start to charge the two switches S3 and S4 in the period will be on simultaneously.

Switching states of suggested chopper are given in Table 2. In this table terms "1" and "0" mean that switch is turned on and off, respectively.
be noted that the DC link consists four capacitors (C1-C4) and reference value, the hysteresis control method is used. It must be noted that the charging capacitor is done by voltage dividing. Therefore voltage of inverter will has only five positive level. For connected to a five level inverter as Fig 4a, then output capacitor voltage balancing. If the proposed chopper is connected to output of inverter Fig 4a. Fig 4b shows a nine level inverter with positive and negative levels.

**IV. CONTROL SYSTEM DESCRIPTION**

In this paper, for the balancing the capacitor voltage at its reference value, the hysteresis control method is used. It must be noted that the DC link consists four capacitors (C1-C4) and charging capacitor is done by voltage dividing. Therefore reference voltage value of each capacitor will be Vdc/4. The capacitor charging produce is as follows:

When the capacitor voltage exceeds from upper band, the capacitor charging is stopped and its extra charge is transferred through the diode. Also when the capacitor voltage is less than the lower band, switch in it’s parallel branches will be turn off and so the capacitor starts to charge. Therefore the capacitor voltage required to scrutiny and their reference values are kept constant. Because of Some reasons such as snaber resistances, asymmetric behavior of components, and switching transients and etc. the Capacitor voltage will be devious from their reference values, in which case the presented control system returns the capacitors voltage to their reference values.

For example, operation in one of case is explained.

Assume, When the capacitor C3 is charged, then capacitor C1 voltage is below the lower limit, then the switch S3 will be off and switch S1 will be on and diode D2 forward bias, so the capacitor C2 can be provide c1 deficiency charge through diode D2 with DC power supply until the capacitor C1 will be charged to requirement value. After this process the control system comeback to the normal operation and controls the capacitors voltage at their reference values, respectively.

In presented topology, each capacitor is charged through DC source, directly. Therefore, the charging process is very fast and the lack of charging and extra charging of capacitors will be negligible. In other word, the voltage ripple of capacitors are not visible. Consequently, the presented topology and control system for voltage balancing have fast dynamic response.

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In the proposed chopper, the capacitors are charged to their order. So the sequences of switching states are based on Table 2. Based on this switching algorithm, the block diagram of proposed control method is shown in Fig 5. It can be seen from this figure implementation of presented control system is very simple.
chopper inductors are taken as \( L_1 = L_2 = L_3 = L_4 = 2 \text{ mH} \) and \( \Delta = 2 \text{ V} \) (\( \Delta \) is the hysteresis band set across \( V_C = 50 \text{ V} \)). All of the applied Capacitors in the chopper circuit are same and are taken as \( C_1 = C_2 = C_3 = C_4 = 330 \mu\text{F} \).

The charging of dc link capacitors (\( C_1 - C_4 \)) to its desired value is evident from Fig. 6(a), 6(b), 6(c) and 6(d), respectively. The dc link capacitor voltages are also equalized in this process.

The afore-presented simulation shown voltages stress on switches \( S_1, S_2, S_3, S_4 \) (Fig 7) and these voltage stresses are reduced to one-quarter and one-tenth.

The nine-level inverter output voltage and load current is shown in Fig(8).
VI. CONCLUSION

This paper has proposed a Parallel Switch Based on Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multilevel Inverter, and they consist of chopper circuit and diode-clamped inverter structures. The structure and the operation principle of this topology are introduced for single-phase mode and simulation results for both of the single-phase and three-phase mode with the asymmetric load have been presented. It requires additional inductors but of reduced voltage rating compared with the conventional chopper and flying-capacitor-based chopper. This topology reduced the device voltage stresses by one-quarter and one-tenth.

The various operating modes of the chopper are described according table 2 to achieve the desired performances.

The chopper circuits are applied to balance the voltage of DC link capacitors with any load conditions, as well as participate in synthesizing the output voltage levels.

REFERENCES