A 0.7 dB Noise Figure UWB CMOS LNA with Reactive Feedback in 0.18µm Technology

Mohammad Reza Salehi, Ebrahim Abiri, Hamed shahraki and Mohammad Sadegh Mirzazadeh

Abstract— In this paper, a very low noise LNA is designed. The LNA is based on reactive feedback and the broadband impedance matching and the flat gain are achieved. Also by using inductive degeneration, a noise less resistance is created. This impedance is used to match the input impedance without increasing the noise figure. The LNA is designed in the standard 0.18 µm CMOS technology. Simulation is performed with Agilent technology advanced designed systems (ADS). The noise figure (NF) is below 0.8dB and input and output reflection coefficient are less than -10dB. Also LNA provides 12dB power gain and consume 11.9mW from a 1.2-V voltage supply.

Keywords— ultra-wideband (UWB); noise figure (NF); low noise amplifier (LNA).

I. INTRODUCTION

In the year of 2002, federal communication commission (FCC) in U.S has putted ultra wideband radio technology in the 3.1-10.6 GHz band frequency. Related standard attracted many attentions, because of low power consumption, high data rate and low cast in communication systems. The ultra-wideband systems are not limited to 3.1-10.6GHz band frequency and are used in 22-29GHz band frequency for UWB radar and also 10-26GHz in metropolitan area network. The LNA is the block entrusted to amplify the weak signal received by the antenna in a reception system. The LNA must have low noise figure, low power and good input and output impedance matching. One of the important topology in LNA to provide input impedance matching and increase power gain is common source (CS)[1]. In this topology, the input signal enters to gate. In this topology, the parasitic capacitances of transistor make the amplifier nonlinear. There are some famous technique to decrease the effect of these parasitic capacitances such as inductive degeneration, resistive feedback and dual reactive feedback. The inductive degeneration technique is achieved by adding an inductor at the source of amplifier[1]. This inductor compensates the effect of gate-source capacitance. Also this inductor provides a noiseless resistance to match the input impedance to the source impedance. The resistive feedback technique is achieved by adding a resistance between gate and drain[2].

This resistance flats the gain and also provides good impedance matching. Usually capacitor is series with the resistance to prevent the effect of resistance on DC bias. But this technique will increase the noise figure (NF) in amplifier.

Another important technique to provide good impedance matching, is dual reactive feedback. In this technique by using the Cgd as a reactive feedback, and adding an inductor at the source of transistor, good impedance matching and flat gain are achieved. Another topology in LNA that provides good impedance matching is common gate (CG) topology. In this topology the impedance matching can easily obtain, because the effect of Cgd can be neglected. Also the input impedance depends on the DC current of transistor. But the power gain in this topology is not sufficient and another stage to increase the gain is required.

Designing of LNA circuit is performed based on three different targets:
1. Low noise
2. Low power consumption
3. High gain

In this paper, a very low noise LNA based on inductive degeneration technique is designed. The LNA consist of two stages. The first stage is in CS topology and provides input impedance matching and power gain. The second stage is in common drain (CD) topology and acts as a buffer stage and provides output impedance matching.

II. CIRCUIT TOPOLOGY AND ANALYSIS

According to Friis law in the cascaded system, total noise figure depend on the gain of first stage extremely.
According to (1), to obtain a low noise figure, gain of the first stage must be maximal. To obtain a good input impedance matching usually common gate topology is used in first stage. But common gate amplifier has a low gain and according to Friis law this topology is not proper for first stage. Another topology that has a high gain is common source. So it can be a good alternative instead of common gate amplifier in first stage. The input stage of designed amplifier is shown in Fig. 2.

\[
F_{\text{tot}} = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \frac{F_4 - 1}{A_1 A_2 A_3} + \ldots
\]

(1)

According to (1), to obtain a low noise figure, gain of the first stage must be maximal. To obtain a good input impedance matching usually common gate topology is used in first stage. But common gate amplifier has a low gain and according to Friis law this topology is not proper for first stage. Another topology that has a high gain is common source. So it can be a good alternative instead of common gate amplifier in first stage. The input stage of designed amplifier is shown in Fig. 2.

As shown in Fig. 2, the inductor L1 and capacitor C1 act as a band pass filter. The capacitor C2 prevents the effect of filter network to the DC bias. The inductor Ls is added to implement the inductive impedance. The small signal of input stage is shown in Fig. 3

\[
Z_{\text{in}}(\omega) = \frac{v_{\text{in}}(\omega)}{i_{\text{in}}(\omega)} = \frac{1}{jC_{\text{gs}} \omega} + j(L_s + L_m)\omega + \frac{g_m}{C_{\text{gs}}} L_s
\]

(3)

As shown in equation 2, a noise less resistance is created. The noiseless resistance depends on the current bias, C_{gs} and the inductor. By choosing proper current bias and inductor, the input impedance matching can be achieved. In this condition, the frequency of input signal must be equal to 4.

\[
\omega = \frac{1}{\sqrt{(L_s + L_m)C_{\text{gs}}}}
\]

(4)

According to the input small signal an equation 3, the power gain is described as below

\[
G_{\text{tot}} \approx \frac{(SL_2 + \frac{1}{SC_{\text{gs}}}) \times 1 + g_m r_d}{SL_2 + \frac{1}{SC_{\text{gs}}} + Z_{\text{in}} \times (1 + g_m r_d) + r_d}
\]

(5)

According to equation 5, to increase the power gain, L_s must decrease. And also L2 must increase.

III. LNA DESIGN

In Fig. 4 the designed proposed LNA is shown. The inductor L1 and capacitor C1 act as a band pass filter and reject the signals which are out of 3.1-12GHZ. Also L1 helps to provide good impedance matching. The capacitor C2 is added to prevent the effect of filter network to the DC bias. The inductor Ls is added to implement the inductive
Degeneration technique to match the input impedance. Also the inductor L2 is added to compensate the capacitive effect of buffer stage. The output impedance matching is provided by adding two inductor L3 and L4, the power supply is 1.2 V and the LNA consume 11.9mW from power supply. In Fig. 5, the power gain of proposed LNA is shown.

As shown in Fig. 5, the LNA provides 12dB power gain. in Fig. 6 the S11 and the S22 of LNA is shown.

As shown in Fig. 6, the LNA has good input and output impedance matching and the S11 and S22 are below -10dB in 4-10.6GHz. In Fig. 7, the noise figure (NF) of proposed LNA is shown.

NF of LNA is 0.2-0.8 dB in band frequency and to evaluate this work using a figure of merit (FOM) defined as:

\[
FOM1 = \frac{\text{GAIN}(dB)}{\text{NF}_{\text{max}}(dB)}
\]

\[
FOM2 = \frac{\text{GAIN}(dB) \cdot \text{BW}(MHz)}{P(mw) \cdot \text{NF}_{\text{max}}}
\]

The performance summery and compression to other CMOS UWB LNA is listed in table. II. Also in table II, the value of proposed LNA is listed.

TABLE I. PERFORMANCE SUMMERY AND COMPRESSION TO OTHER CMOS UWB LNA

<table>
<thead>
<tr>
<th>Devices</th>
<th>L1</th>
<th>L2</th>
<th>C1</th>
<th>C2</th>
<th>R1</th>
<th>L3</th>
<th>Ls</th>
<th>L4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>1nH</td>
<td>4nH</td>
<td>1nF</td>
<td>240nF</td>
<td>5kΩ</td>
<td>4nH</td>
<td>13nH</td>
<td>8nH</td>
</tr>
</tbody>
</table>

| 1 | 7 | 11.5 | < -9 | 9 | 3.3-11 | 1.64 | 642 |
| 2 | 5.3 | 12.1 | < -10 | 12.6 | 1-10 | 2.28 | 850 |
| 3 | 7.2 | 12.5 | < -9 | < 7 | 18.3 | 3-11 | 1.73 | 352 |
| 4 | 9.2 | 10.4 | < -10 | < 10 | < 9.4 | 9 | 2.4-9.5 | 1.13 | 314 |
| 5 | 6.5 | 12.4 | < -10 | 12 | 0.4-10 | 1.90 | 747 |
| 6 | 4.7 | 13.1 | < -8 | < 9.4 | 10.7 | 0.6-10 | 2.28 | 1460 |
| this work | .7 | 12 | < -10 | 11.9 | 4-10 | 17 | 7560 |
As shown in table. I, the FOM in this work is larger than the other LNAs.

IV. CONCLUSION

A broad band LNA for UWB application has been introduced, analyzed and simulated. In this work by using, reactive feedback and coupled inductors a LNA with very low noise figure is designed. The LNA has good input and output impedance matching and provides 12dB power gain from a 1.2V supply power.

REFERENCES