Control Method of a Parallel-Connected Ring-Type Converter to Reduce Parasitic Power Losses

Kei Eguchi, Shinya Terada, Ichirou Oota, and Hirofumi Sasaki

Abstract—To reduce parasitic power losses, a parallel-connected ring-type converter using a charge reusing technique is introduced in this paper. Although the conventional ring-type converter consumes the electric charge in stray parasitic capacitances idly, the proposed parallel-connected converter reuses a part of the electric charge in stray parasitic capacitances. Therefore, the proposed converter can realize higher power efficiency than the conventional parallel-connected ring-type converter, because the proposed converter can reduce parasitic power losses. Concerning the simplest example of the proposed converter, simulation program with integrated circuit emphasis (SPICE) simulations and theoretical analysis were performed to clarify characteristics. The result of SPICE simulations showed that the proposed converter can greatly improve power efficiency when the output load is a large value. Furthermore, handy theoretical formulas to estimate the maximum efficiency were obtained by the theoretical analysis. The results of the theoretical analysis corresponded well with the SPICE simulated results.

Keywords—DC-DC converters, step-up/step-down conversion, charge reusing techniques, stray parasitic capacitances.

I. INTRODUCTION

In the development of mobile equipments, the need of a small DC-DC converter is increasing. To realize small DC-DC converters, the switched capacitor (SC) power converter [1]-[5] is one of the most promising converters, because the SC power converter can be implemented into an integrated circuit (IC) chip [1]. Among others, we focus on a ring-type power converter [3]-[5]. Unlike charge pump converters [1] and Fibonacci-type converters [2], the ring-type converter can achieve step-up/step-down conversion by controlling the timing of clock pulses. In other words, the ring-type converter can provide flexible output voltages. However, in the design of the conventional ring-type converter, the energy loss due to parasitic capacitances has not been taken into account [3]-[5]. Although the power efficiency of the SC power converter consisting of discrete circuit components is mainly limited by capacitor charging and discharging losses and resistive conduction losses, the energy loss due to stray parasitic capacitances cannot be ignored in integrated SC converters.

In this paper, in order to develop the integrated SC DC-DC converter which can offer enough power to output loads, we propose a parallel-connected ring-type converter using a charge reusing technique. In the conventional ring-type converter [3]-[5], the electric charge in stray parasitic capacitances is consumed idly. On the other hand, by connecting the stray parasitic capacitances at the end of each clock cycle, the proposed converter reuses a part of the electric charge in stray parasitic capacitances. Therefore, the proposed converter can reduce parasitic power losses by the equalization process of the stray parasitic capacitances. Furthermore, the proposed parallel-connected converter can achieve small ripple noise as well as large output currents. To confirm the validity of the proposed technique, simulation program with integrated circuit emphasis (SPICE) simulations and theoretical analysis are performed.

Fig. 1 Conventional ring-type converter

Kei Eguchi is with the Department of Information Electronics, Fukuoka Institute of Technology, 3-30-1 Wajirohigashi, Higashi-ku, Fukuoka, Japan (phone:+81-92-606-3137; fax:+81-92-606-6726; e-mail:eguchi@fit.ac.jp).
Shinya Terada is with the Department of Information and Communication, Kumamoto National College of Technology, 2659-2, Suya, Koushi, Kumamoto, Japan (e-mail:terada@ee.knct.ac.jp).
Ichirou Oota is with the Department of Information and Communication, Kumamoto National College of Technology, 2659-2, Suya, Koushi, Kumamoto, Japan (e-mail:oota-i@tc.knct.ac.jp).
Hirofumi Sasaki was with the School of Industrial Engineering, Tokai University, 9-1-1 Toroku, Kumamoto, Japan. He is now with Tokai University, 9-1-1 Toroku, Kumamoto, Japan. (e-mail:hssasaki@ktmail.tokai-u.jp).
II. CIRCUIT STRUCTURE

A. Conventional Ring-Type Converter

Fig.1 shows the conventional ring-type converter [3]-[5]. The conventional converter realizes \( s/r \) (where \( i = 1, 2, \ldots, N \) and \( s = 1, 2, \ldots, N \)) step-up/step-down conversion. In Fig.1, clock pulses for the power switch \( S_{ij}, j = 1, 2, \ldots, N \) are non-overlapped \( N \)-phase pulses \( \Phi_{ij} \), and clock pulses for \( S_{ij} \) are set to inverted pulses of \( \Phi_{ij} \). According to the conversion ratio \( s/r \), the power switches \( S_{ij} \) and \( S_{ij} \) are driven by clock pulses obtained by shifting the clock pulse \( \Phi_{ij} \) cyclically. In other words, by controlling the timing of \( \Phi_{ij} \) and \( \Phi_{ij} \), the conversion ratio is determined.

In the previous studies [3]-[5], the existence of stray parasitic capacitances has not been taken into account in the design of the ring-type converter. When the SC power converter is integrated into an IC form, stray parasitic capacitances exist as shown in Fig.2, where \( C_t \) denotes the stray parasitic capacitance between top plate and substrate and \( C_b \) denotes the stray parasitic capacitance between bottom plate and substrate. In the conventional converter, the electric charge \( Q \) charged in \( C_b \) is consumed idly when \( C_j \) is grounded via \( S_{ij} \).

B. Proposed Converter

To reduce the energy loss due to stray parasitic capacitances, we proposed a new ring-type converter. To help readers’ understanding, let us consider the simplest example of the proposed converter. Fig. 3 shows the simplest example of the proposed converter. As Fig.3 shows, the proposed converter consists of two ring-type converters connected mutually through the power switch \( S_5 \).

Tables I and II show the timing of clock pulses. The proposed converter shown in Fig.3 achieves the 2x stepped-up conversion and the 1/2 stepped-down conversion. As shown in Fig.3, the power switch \( S_5 \) is turned on at the end of each clock cycle. In this timing, the electric charges stored in the stray parasitic capacitances \( C_b \) are equalized through the power switch \( S_5 \). Therefore, due to the equalization process of the electric charge in \( C_b \), the power dissipation of the input can be reduced.

The properties of the proposed converter will be analyzed in the following section.

III. THEORETICAL ANALYSIS

Concerning power efficiency and output voltage, the theoretical analysis is performed in this section. To evaluate the maximum power efficiency, we assume that 1. Parasitic elements are negligibly small and 2. Time constant is much larger than the period of clock pulses.

A. Step-Up Conversion

Fig. 4 shows the instantaneous equivalent circuits of the proposed converter, where \( R_{in} \) denotes the on-resistance of the power switch. In Fig.4, \( State-T_1 \) is a charging process, \( State-T_3 \) is a transferring process, and \( State-T_2 \) and \( State-T_4 \) are charge reusing processes. In Fig.4, the differential value of the electric charge in capacitor \( C_k \) (\( k = 1, 2, 3, 4 \)) satisfies

\[
\sum_{i=1}^{4} \Delta q_i = 0,
\]

where

\[
T = \sum_{i=1}^{4} T_i, \quad T_1 = T_3 = T_s, \quad \text{and} \quad T_2 = T_4 = \gamma T.
\]
In (1), $\gamma (\leq 0.5)$ is a constant parameter and $\Delta q_{i}^{k}$ ($i=1, 2, 3, 4$) denotes electric charges in the case of State-$T_i$. In the case of State-$T_i$, the differential values of electric charges in the terminal $V_{in}$ and terminal $V_{out}$, $\Delta q_{Ti,Vin}$ and $\Delta q_{Ti,Vout}$, are expressed by the following equations:

**State-$T_1$:**

\[
\Delta q_{T_1,Vin} = \Delta q_{T_1} - \Delta q_{T_1}^2 + \Delta q_{T_1}^3 + \Delta q_{T_1}^4,
\]
\[
\Delta q_{T_1,Vout} = \Delta q_{T_1}^3 + \Delta q_{T_1}^4,
\]
\[
\Delta q_{T_1}^2 = \Delta q_{T_1}^3,
\]
\[
\Delta q_{T_1} = \Delta q_{T_1}^4.
\]

and

\[
\Delta q_{T_1}^2 = \Delta q_{T_1}^4 = \Delta q_{T_1}^5 = \Delta q_{T_1}^6 = 0.
\]

**State-$T_2$:**

\[
\Delta q_{T_2,Vin} = \Delta q_{T_2,Vout} = 0
\]

and

\[
\Delta q_{T_2}^2 = \Delta q_{T_2}^3 = \Delta q_{T_2}^4 = 0.
\]

Furthermore, we have the following conditions:

\[
\Delta q_{T_1}^2 = \Delta q_{T_1}^3 = \Delta q_{T_1}^4 = \Delta q_{T_1}^5 = \Delta q_{T_1}^6 = 0.
\]
general equivalent circuit of SC power converters, the consumed energy $W_T$ is defined by

$$W_T = \sum_{i=1}^{4} W_{T_i} = \left( \frac{\Delta q_{\text{out}}}{T} \right)^2 \cdot R_{\text{SC}} \cdot T,$$

(11)

where $R_{\text{SC}}$ is called the SC resistance. Therefore, from (10) and (11), the SC resistance in the case of the step-up conversion is expressed as

$$R_{\text{SC}} = \frac{7R_{\text{on}}}{2(1-2\gamma)}.$$  

(12)

By combining (7) and (12), the equivalent circuit in the case of the step-up conversion can be expressed by the following determinant:

$$\begin{vmatrix} V_{\text{out}} \\ T_{\text{in}} \end{vmatrix} = \begin{bmatrix} \frac{1}{2} & 0 \\ 0 & \frac{1}{2} \end{bmatrix} \begin{bmatrix} R_{\text{SC}} \\ 0 \end{bmatrix} \begin{bmatrix} V_{\text{out}} \\ T_{\text{in}} \end{bmatrix},$$

(13)

because the equivalent circuit of the SC power converters can be expressed by the determinant using the Kettenmatrix. Finally, from (13), the power efficiency and the output voltage of the proposed converter are obtained as

$$\eta = \frac{(I_{\text{out}})^2 R_L}{(I_{\text{out}})^2 R_{\text{SC}} + (I_{\text{out}})^2 R_L} = \frac{R_L}{R_{\text{SC}} + R_L},$$

and

$$V_{\text{out}} = \frac{R_L}{R_{\text{SC}} + R_L} \times (2V_{\text{in}}),$$

(14)

where $R_L$ denotes the output load. As (12) and (14) show, the power efficiency decreases with increase in $R_{\text{out}}$ and $\gamma$.

### B. Step-Down Conversion

In the case of $\text{State-T}_1$, the differential values of electric charges in the terminal $V_{\text{in}}$ and terminal $V_{\text{out}}$ are expressed by the following equations.

**State-T$_1$:**

$$\Delta q_{T_1, V_{\text{in}}} = \Delta q_{T_1}^1,$$

$$\Delta q_{T_1, V_{\text{out}}} = \Delta q_{T_1}^1 - \Delta q_{T_1}^2 - \Delta q_{T_1}^3 + \Delta q_{T_1}^4,$$

$$\Delta q_{T_1}^1 = \Delta q_{T_1}^4,$$

and

$$\Delta q_{T_1}^2 = \Delta q_{T_1}^3.$$

(15)

**State-T$_2$:**

$$\Delta q_{T_2, V_{\text{in}}} = \Delta q_{T_2}^1,$$

$$\Delta q_{T_2, V_{\text{out}}} = -\Delta q_{T_2}^1 + \Delta q_{T_2}^2 + \Delta q_{T_2}^3 - \Delta q_{T_2}^4,$$

$$\Delta q_{T_2}^1 = \Delta q_{T_2}^4,$$

and

$$\Delta q_{T_2}^2 = \Delta q_{T_2}^3.$$

(16)

**State-T$_3$:**

$$\Delta q_{T_3, V_{\text{in}}} = \Delta q_{T_3}^1,$$

$$\Delta q_{T_3, V_{\text{out}}} = -\Delta q_{T_3}^1 + \Delta q_{T_3}^2 + \Delta q_{T_3}^3 - \Delta q_{T_3}^4,$$

$$\Delta q_{T_3}^1 = \Delta q_{T_3}^4,$$

and

$$\Delta q_{T_3}^2 = \Delta q_{T_3}^3.$$

(17)

**State-T$_4$:**

$$\Delta q_{T_4, V_{\text{in}}} = \Delta q_{T_4}^1,$$

$$\Delta q_{T_4, V_{\text{out}}} = -\Delta q_{T_4}^1 + \Delta q_{T_4}^2 + \Delta q_{T_4}^3 - \Delta q_{T_4}^4,$$

$$\Delta q_{T_4}^1 = \Delta q_{T_4}^4,$$

and

$$\Delta q_{T_4}^2 = \Delta q_{T_4}^3.$$

(18)

By substituting (1), (6), (15), (16), (17), and (18) for (7), we have the following relation between the average output current and the average input current:

$$I_{\text{out}} = \frac{2R_{\text{on}}}{T_i} \left( \Delta q_{T_1}^1 \right)^2 + \frac{2R_{\text{on}}}{T_i} \left( \Delta q_{T_2}^1 \right)^2 + \frac{R_{\text{on}}}{T_i} \left( \Delta q_{T_3}^1 - \Delta q_{T_4}^2 \right)^2 + \frac{2R_{\text{on}}}{T_i} \left( \Delta q_{T_2}^1 \right)^2 + \frac{R_{\text{on}}}{T_i} \left( \Delta q_{T_3}^1 - \Delta q_{T_4}^2 \right)^2,$$

(19)

Next, the consumed energy in the case of the step-down conversion can be expressed as

$$W_T = \sum_{i=1}^{4} W_{T_i},$$

(20)

where

$$W_{T_i} = W_{T_i},$$

$$= \frac{R_{\text{on}}}{T_i} \left( \Delta q_{T_1}^1 \right)^2 + \frac{2R_{\text{on}}}{T_i} \left( \Delta q_{T_2}^1 \right)^2 + \frac{R_{\text{on}}}{T_i} \left( \Delta q_{T_3}^1 - \Delta q_{T_4}^2 \right)^2 + \frac{2R_{\text{on}}}{T_i} \left( \Delta q_{T_2}^1 \right)^2 + \frac{R_{\text{on}}}{T_i} \left( \Delta q_{T_3}^1 - \Delta q_{T_4}^2 \right)^2,$$

and

$$W_{T_i} = 0.$$

Therefore, equation (20) can be rewritten as

$$W_T = 2W_{T_i} - \frac{7R_{\text{on}}}{8(1-2\gamma)} \left( \Delta q_{V_{\text{out}}} \right)^2.$$  

(21)

From (11) and (21), the SC resistance is expressed as

$$R_{\text{SC}} = \frac{7R_{\text{on}}}{8(1-2\gamma)}.$$  

(22)

Finally, the power efficiency and the output voltage can be expressed by

$$\eta = \frac{R_L}{R_{\text{SC}} + R_L}$$

and

$$V_{\text{out}} = \frac{R_L}{R_{\text{SC}} + R_L} \times \left( \frac{V_{\text{in}}}{2} \right),$$

(23)

respectively.

### IV. SIMULATION

To confirm the validity of theoretical analysis, the properties of the proposed converter are investigated by SPICE simulations, where $V_{\text{in}} = 3.7V$, $C_1 = C_2 = C_3 = C_4 = 200nF$, $R_{\text{on}} = 10\Omega$ and $T = 100ns$.

Fig. 5 shows the simulated maximum power efficiency as a function of $\gamma$. In the SPICE simulation of Fig.5, the stray parasitic capacitances were set to zero in order to evaluate the maximum power efficiency. As Fig.5 shows, the theoretical results correspond well with the SPICE simulated results. Consequently, the validity of the theoretical analysis was confirmed. Furthermore, as Fig.5 shows, the power efficiency
decreases with increase in the parameter $\gamma$. Therefore, according to the value of stray parasitic capacitances, the parameter $\gamma$ must be determined.

Fig. 6 shows the comparison of the simulated power efficiency between the proposed converter and the conventional parallel-connected ring-type converter. In the SPICE simulation of Fig.6, the stray parasitic capacitance $C_t$ and $C_b$ were set to the same value. Of course, the value of the stray parasitic capacitance changes according to a device process and the type of the capacitor. As Fig.6 shows, the proposed converter can improve power efficiency when $R_L$ is a large value. Concretely, in the case of the step-down conversion, the proposed converter can improve the power efficiency by about 10% from the conventional converter when the output load $R_L$ is 1kohm and $\alpha=\beta=0.1\%$.

V. CONCLUSION

In this paper, a parallel-connected ring-type converter has been proposed to reduce parasitic power losses. The result of SPICE simulations showed that the proposed converter can reduce the parasitic power losses when the output load $R_L$ is a large value. Concretely, about 10% of the power efficiency was improved by the proposed technique when the output load $R_L$ is 1kohm. Furthermore, the maximum power efficiency obtained by the theoretical analysis corresponded well with the SPICE simulated results. Therefore, the formulas obtained by the theoretical analysis will be helpful to design the proposed converter.

The IC implementation of the proposed converter is left to a future study.

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REFERENCES


Kalman Filter Implementation on an Accelerometer sensor data for three state estimation of a dynamic system

Toshak Singhal, Akshat Harit, and D N Vishwakarma

Abstract—Kalman Filter is used in many system estimation applications like state estimation, digital signal processing, sensor integration, Navigational Systems, etc. Kalman Filter is frequently used for the purpose of filtering accelerometer data to give position and velocity coordinates. This paper presents a Kalman filter implementation using a system model based on constant acceleration and analyzes its performance for different use cases. Furthermore, relation of $q$ and $R$ parameters of Kalman filter is also presented with respect to errors in measurements. The paper also discusses the different implementations that can be used for optimally predicting acceleration along with velocity and position.

Keywords—Kalman Filter, State Estimation, Kalman Filter error Analysis, Accelerometer sensor

I. INTRODUCTION

Kalman Filter is a digital filter used to filter noise on a series of measurements observed over a time interval. Recent advancements have been made and various successive filters such as Extended Kalman Filter (EKF) and Unscented Kalman Filter (UKF) have been derived from it. It is an algorithm used to solve the linear quadratic Gaussian (LQG) estimation problem. It operates recursively on the data stream of a dynamic system to give an optimum estimate of the current system state. It has numerous applications in various fields like Power System state estimation [2][3], Aircraft Guidance and navigational control systems. The Kalman filter algorithm is based on two steps; first the prediction step in which the current estimate of state variables, with random noise included is given. The prediction step only involves data measurement before the time at which system state is to be calculated. These estimates are used along with the measurement, with random Gaussian noise, to give the correct state of the system. The algorithm works by using a weighted average model on the predicted value and the current value. The more certain measurement is given more weight. The filter works in the discrete time domain. Implementations are available for continuous time version, called Kalman-Bucy filter. Another variant, the Unscented Kalman Filter (UKF) [4] is used when state transition and observation models are highly non-linear i.e. cases in which EKF gives poor performance. Also Kalman filter has been proven to give excellent results in the sensor data fusion [5] sometimes along with Fuzzy logic. Kalman filter in sensor data fusion treats one sensor data as measurement and other as prediction. It has been very frequently used to integrate GPS (Global Positioning System) and IMU (Inertial Measurement Unit) unit employed in both Airborne and terrestrial automated vehicles.

II. NOMENCLATURE

$x_k$ System State Matrix
$w_k$ Process Noise
$z_k$ Measurement Result Matrix
$v_k$ Measurement Noise
$\Phi_k$ State Transition Matrix
$P_k$ State Error Covariance Matrix
$H_k$ Measurement transition Matrix
$K_k$ Kalman Gain
$Q$ Process Noise Covariance
$R$ Measurement Noise Covariance
$E$ Expectation Operator

III. SYSTEM MODEL

System modelled in this paper is a three state system with acceleration, velocity and position being the three states. The process noise added is White Gaussian noise with signal to noise ratio equal to -2. Similarly, the measurement noise is also White Gaussian noise with signal to noise ratio equal to -2. Now system equations can be given as

$$x_{k+1} = x_k + w_k$$  \hspace{0.5cm} (1)

$$z_k = x_k + v_k$$  \hspace{0.5cm} (2)